GC-IP201 / GC-IP201(B)

Datasheet

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Revision History

Date	Revision	Change(s)
26/03/2012	0.1	First Version / preliminary version
19/09/2012	0.2	Update for Engineering Samples
12/10/2012	0.3	Pin list and Block diagram new
19/03/2013	1.0	Updated chapter EEPROM
17/10/2014	1.1	Update of the input signal parameters and maximum input signal frequency Update of the electrical specification parameters
25/01/2017	1.2	change document layout according to AMAC CI

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1 Overview

The interpolation circuits GC-IP201 and GC-IP201B serve to increase the resolution of incremental position and angular measuring systems with sinusoidal output signals. The input signals are subjected to an AMAC-specific internal gain and offset control, which leads to a correction of amplitude and zero position. Additionally, the phase deviation of the input signals can be corrected statically via a digital potentiometer. The signal period is divided up to 256 times. The position or angle value, which is output to the preprocessing components via its fast SPI interface, its SSI interface, its BiSS interface (GC-IP201B only) or via standard ABZ square wave signals.

The interpolation circuits GC-IP201(B) are suitable for input and output interfaces with 3.3V. These ICs comprise three instrument amplifiers with adjustable gain factors. Incremental encoders with voltage interface as well as measuring bridges can be connected directly to these interpolation ICs. Sensors with current interface and photodiode-arrays are adapted by a simple external circuit. The GC-IP201(B) can be used with both single-ended and differential signals. The noise of the sensor signals is reduced by a switching analog filter. Additionally, a digital hysteresis can suppress the edge noise of the output signals at low input frequencies and at standstill. Thus, a subsequently connected interpolation counter works properly even in case of short-time disturbances. The quality of the signals issued by the sensors is monitored in these ICs. For that purpose it is possible to activate 9 sources separately, which are producing an error signal.

The propagation delay of the circuit is 2.4µs only. Due to the implemented multi-stage triggering, the internal clock as well as the SPI interface with up to 25MHz clock frequency, the interpolation ICs GC-IP201(B) are the ideal choice for use in fast multi-channel controllers or control systems. The four integrated output interfaces (ABZ/SPI/SSI/BiSS) and further features such as the multi-stage trigger signal processing, integrated timer, integrated multi-turn counter, the processing of distance coded reference marks, the possibility to adjust the reference mark as well as adjustment and storage of the zero position make these ICs suitable for direct use of the ICs in industrial controls or in fast multi-channel positioning measuring systems. With these features the ICs are suitable for absolute positioning measuring systems.

The GC-IP201(B) can be configured specifically to the particular application via an internal EEPROM, configuration pins or via the serial interface (SPI/BISS).

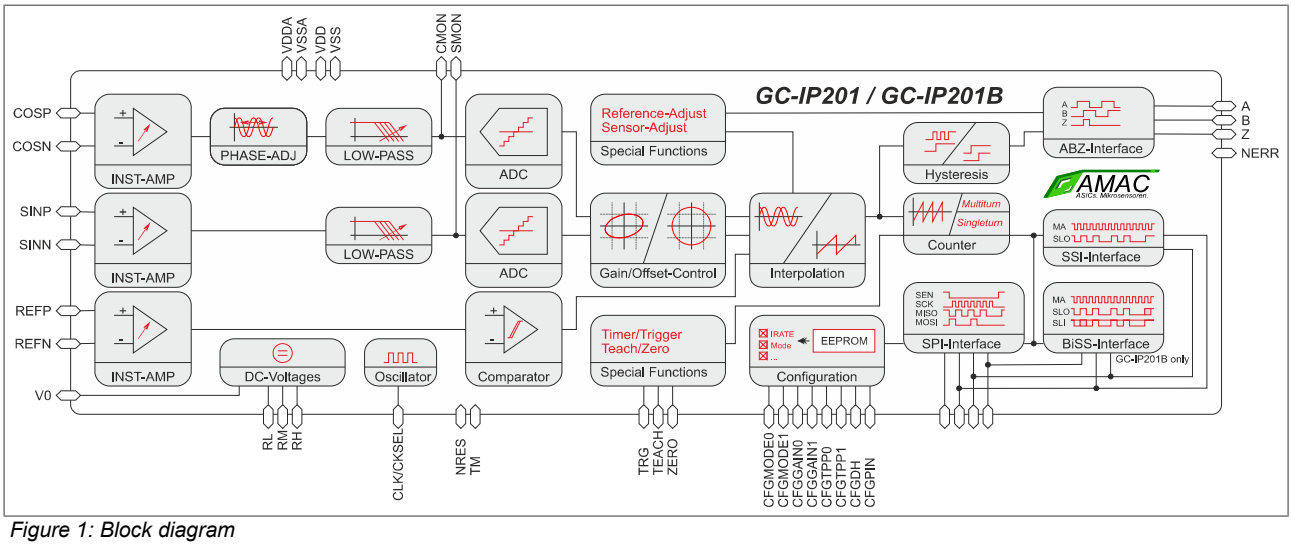


Figure 1: Block diagram

2 Features

Interfaces	
Analog input	- Sine- / Cosine- / Reference signal; differential or single-ended - Nominal amplitude configurable to 660mVpp / 330mV$_{pp}$ / 160 mV$_{pp}$ / 50mV$_{pp}$ (corresponds 1V$_{pp}$ / 500mV$_{pp}$ / 240mV$_{pp}$ / 80mV$_{pp}$ at 5V systems) - Maximum input frequency 440kHz for all resolutions (410 kHz with internal controller enabled)
ABZ	- 90°-square wave sequences (A/B/Z) - Adjustable width of the index signal Z of ¼ or 1 period A/B - Error signal - Interrupt signal for µC - Additional signals for sensor adjustment
SPI	- 30 Bit counting value / 16 Bit multi-turn value - Data rate up to 500 000 measuring values/s - 9 Bit signal monitoring - Standard SPI compatible: 16 Bit, MSB first, up to 25MHz - Signal filter for noise suppression
SSI and BiSS	- Up to 30 Bit counting value / 16 Bit multi-turn value - 2 Bit signal monitoring - Gray code / binary code - Adjustable timing - SSI ring mode
Further inputs	- Trigger signal for measurement value storage - Zero-signal and Teach-signal for adjusting and storage of the sensor zero position
Configuration options	- Internal EEPROM - Configuration inputs - Serial interface (SPI/BiSS)
Interpolation / Signal Processing	
Interpolation rates	256, 200, 160, 128, 100, 80, 64, (50), 40, 32, (25), 20
Signal correction	- AMAC-specific digital offset regulation, regulation range ±15% of the nominal amplitude - AMAC-specific digital amplitude regulation, regulation range factor 60% ... 120% nominal amplitude - Digital 15 step potentiometer for phase correction; adjusting range ±5° or ±10° - Monitoring and evaluation of the input signal quality - Programmable reaction to sensor errors
Suppression of disturbances	- Adjustable low pass filter 10kHz, 75kHz, 200kHz, 450kHz - Digital hysteresis for edge noise suppression at the output (0 … 7) - Adjustable minimum edge distance (band width limitation) at the output
Reference signal processing	- Adjustable reference point position 32 steps 0° … 360° - Identification of the optimum reference position via SPI/BiSS or additional signals - Processing of distance coded reference marks - Measurement value trigger at reference point position
Others	- 2-step measurement value trigger - Programmable timer (3.2µs … 420ms) - Delay time between sampling and measurement value constant 2.4µs for all resolutions - Multi-turn counter
Main Features	
Package	QFN40 (6 mm x 6 mm)
Power supply voltage	3.3V
Temperature range	-40°C … 150°C
Interface frequency	SPI 25MHz, BiSS 10MHz, SSI 5MHz

3 Ordering Information

Product Type	Description	Article Number
GC-IP201	Interpolation circuit GC-IP201, QFN40	PR-44201-00
GC-IP201B	Interpolation circuit GC-IP201B incl. BiSS interface, QFN40	PR-44202-00
GC-LS	4-channel analog level-shifter 5V to 3.3V	PR-44500-00
GP201(B)	Demoboard for interpolation circuit GC-IP201(B)	PR-44200-00
USB to SPI Adapter	USB-Adapter for SPI interface	PR-44025-10

4 Application Overview

Table 1: Application overview

Signal Form (Sensor)	Application GC-IP201(B)
Sine, voltage	Direct connection of GC-IP201(B) to the sensor
Sine, current	Additional resistor circuit required
Reference signal	Direct connection of GC-IP201(B) to the sensor
Square wave	ICs basically not recommended
Signal Specification (Sensor)	**Application GC-IP201(B)**
$1V_{pp}$ nominal	Direct connection via GC-LS or via special resistor circuit
$660mV_{pp}$ nominal	Direct connection of GC-IP201(B) to the sensor
$330mV_{pp}$ nominal	Direct connection of GC-IP201(B) to the sensor
$160mV_{pp}$ nominal	Direct connection of GC-IP201(B) to the sensor
$80mV_{pp}$ nominal	Direct connection via GC-LS or via special resistor circuit
$50mV_{pp}$ nominal	Direct connection of GC-IP201(B) to the sensor
$2V_{pp}$ nominal	Additional resistor circuit required
Differential signal, DC voltage level 0.82V ... 1.8V	Direct connection of GC-IP201(B) to the sensor
Single-ended, DC voltage source inside the sensor	Direct connection of GC-IP201(B) to the sensor
Single-ended, no DC voltage source inside the sensor	Direct connection of GC-IP201(B) to the sensor or via special resistor circuit
Photo diodes $0.5\mu A_{pp}$	Additional resistor circuit required
Photo diodes $11\mu A_{pp}$ ...$16\mu A_{pp}$	Additional resistor circuit required
Resistive sensor bridge (magnetic sensors)	Direct connection of GC-IP201(B) to the sensor
Floating amplitude of the sensors	GC-IP201(B) contains amplitude regulation
No correction of sensor signal offset	GC-IP201(B) contains offset regulation
No correction of sensor signal phase	GC-IP201(B) contains potentiometer for phase adjustment
Fluctuating reference signal position	GC-IP201(B) contains possibility for zero position adjustment
Distance coded reference mark	Special trigger mode for GC-IP201(B) in case of connection via SPI
Processing Electronic	**Application GC-IP201(B)**
Output to µController/DSP/FPGA	Connection via SPI interface
Output to external interpolation counter	Connection via ABZ interface
Output to industrial controls	Connection via SSI, BiSS or ABZ interface
System contains additional channels	Simultaneous use at one SPI/BiSS-bus only possible
Real time application / equidistant sampling	2.4µs constant propagation time, trigger or timer use
IC configuration	Internal EEPROM, all registers configureable via SPI and BiSS
Signal specification LVCMOS	Input / output directly usable
Signal specification RS422	Line driver required
Multi-turn counter required	Connection via SPI, SSI, BiSS
Maximum Signal Frequency	
Rotary encoders:	f_{max} = (revolution/minute) · (signal periods/revolution) / 60
Linear encoders:	f_{max} = (v_{MAX} [in m/s] / (signal period [in mm]) · 1000
f_{max} < 440kHz	Interpolation rates up to 256 via SPI/SSI/BiSS with internal controller disabled
f_{max} < 410kHz	Interpolation rates up to 256 via SPI/SSI/BiSS with internal controller enabled
f_{max} < 40MHz / Interpolation rate	For ABZ output
Maximum counter frequency at ABZ known	GC-IP201(B) adaptation via `CFGTPP` possible
Package	
Package	QFN40, outer dimension 6 mm x 6 mm
Minimum circuit	7 Block-C, 2 pull-up resistors, optional: RS422-driver

5 Package

Table 2: Pin list QFN40

Pin	Name	Type	Description
1	VDDA	Power	Power supply voltage analog +3.3V
2	V0	Output analog (Buffer)	Mean voltage for sensor use
3	RL	Analog	ADC reference voltage 0.625V – C external
4	RH	Analog	ADC reference voltage 1.575V – C external
5	RM	Analog	ADC reference voltage 1.1V – C external
6	VSSA	Power	Analog ground
7	VDDA	Power	Power supply voltage analog +3.3V
8	OUTR_tst	Output analog	Test output
9	REFP	Input analog	Input reference positive
10	REFN	Input analog	Input reference negative
11	COSP	Input analog	Input cosine positive
12	COSN	Input analog	Input cosine negative
13	SINP	Input analog	Input sine positive
14	SINN	Input analog	Input sine negative
15	CFGTPP<0>/HWA<0>	Input digital / Pull down	Configuration interval time / hardware address
16	CFGTPP<1>/HWA<1>	Input digital / Pull down	Configuration interval time / hardware address
17	CFGMODE<1>/Zero	Input digital / Pull up	Configuration mode ABZ / trigger pulse for counter reset
18	CFGMODE<0>/Teach	Input digital / Pull up	Configuration mode ABZ / trigger pulse for counter value storage
19	NRES	Input / Output digital /Open-Drain/ Pull-Up	Reset
20	CLK/CKSEL	Input digital / Pull down	Clock or selection internal RC oscillator at permanent Low
21	NERR	Output digital / Open-Drain	Error signal / signal for sensor adjustment, **external Pull up required**
22	Z	Output digital[1)]	Output zero (index) signal / signal for sensor adjustment
23	B	Output digital[1)]	Incremental output B / signal for sensor adjustment / sample signal
24	A	Output digital[1)]	Incremental output A / signal for sensor adjustment / Interrupt signal
25	VSS / VSSIO	Power	Digital ground
26	VDD / VDDIO	Power	Power supply voltage digital +3.3V
27	MISO/SLO	Output digital / Open-Drain	SPI/BiSS/SSI: Data output GC-IP201(B), **external Pull up required**
28	SCK/MA	Input digital / Pull down	SPI/BiSS/SSI: Clock
29	MOSI/SLI	Input digital / Pull down	SPI/BiSS: Data input GC-IP201(B)
30	SEN	Input digital / Pull up	SPI: Enable / during Reset: configuration SPI / BiSS or SSI
31	TM	Input digital / Pull down	Test mode; connection to VSS
32	CFGPIN	Input digital / Pull up	Configuration selection by EEPROM or by Pin
33	CFGGAIN<1>/HWA<3>	Input digital / Pull down	Configuration GAIN and nominal amplitude / hardware address
34	CFGGAIN<0>/HWA<2>	Input digital / Pull down	Configuration GAIN and nominal amplitude / hardware address
35	VSS	Power	Digital ground
36	VDD	Power	Power supply voltage digital +3.3V
37	CFGDH/TRG	Input digital / Pull up	Configuration digital hysteresis / trigger input
38	CMON	Output analog	Output instrumentation amplifier cosine
39	SMON	Output analog	Output instrumentation amplifier sine
40	VSSA	Power	Analog ground
EXPOSED	VSS	Package	Digital ground

[1)] The status of the pins A, B and Z can be Tristate (optional) in error case.

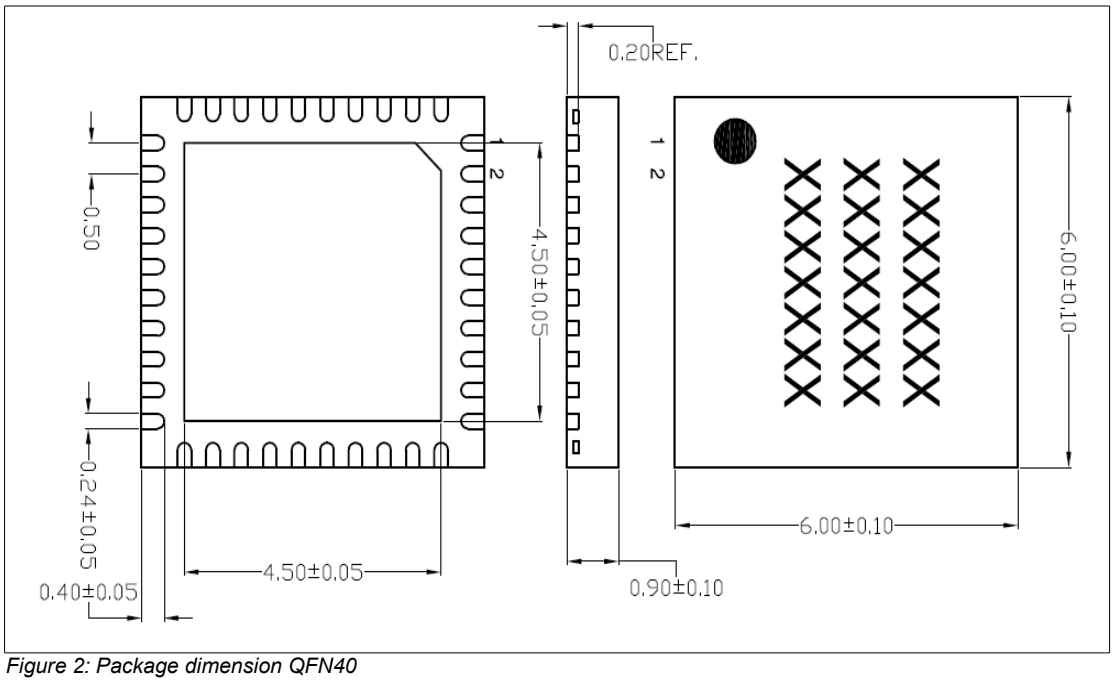


Figure 2: Package dimension QFN40

6 Start up Behaviour / Configuration Options

6.1 Reset

After reset, the GC-IP201(B) selects the digital interface (SPI or SSI/BiSS) according to the input pins and all registers are initialised with their default values. The configuration values are read in from the internal EEPROM or from the configuration inputs. The data of the internal EEPROM is used if valid data is stored at the EEPROM address 0x00 and Low-level at the input pin `CFGPIN`. Depending on the selected interface, the EEPROM, as well as the configuration mode, all double use pins are switched. During the complete reset process the outputs `NERR` or `MISO` are Low. Until then, the serial interfaces may not be active. After complete initialisation, the IC configuration can be changed via the serial interfaces SPI or BiSS at any time. The following tables describe all the required configurations during the reset process.

Table 3: Oscillator configuration

Oscillator	Pin CLK / CKSEL	Frequency
Internal	DVSS	Approx. 40MHz
External	Clock	4MHz … 40MHz

Table 4: Serial Interface selection GC-IP201

Interface	SEN Reset value	BIT SSI [1)]	Pin MISO / SLO	Pin MOSI / SLI	Pin SCK	Pin SEN	Ready-Signal
SPI	1	any	SPI-MISO	SPI-MOSI	SPI-SCK	SPI-SEN	at MISO
SSI	0	any	SSI-DATA	-	SSI-MA	0	at NERR

[1)] Register CFG3 / Bit 15

Table 5: Serial Interface selection GC-IP201B

Interface	SEN Reset value	BIT SSI [1)]	Pin MISO / SLO	Pin MOSI / SLI	Pin SCK	Pin SEN	Ready-Signal
SPI	1	any	SPI-MISO	SPI-MOSI	SPI-SCK	SPI-SEN	at MISO
SSI	0	1	SSI-DATA	-	SSI-MA	0	at NERR
BiSS	0	0	BiSS-SLO	BiSS-SLI	BiSS-MA	0	at NERR

[1)] Register CFG3 / Bit 15

Table 6: Configuration source selection

CFGPIN Reset value	Content EEPROM Address 0x00	Configuration	Configuration pin regarding table 7
1	any	regarding Table 9 (Pin)	For configuration / hardware address = 0000
0	unequal 0x134A	regarding Table 9 (Pin)	For configuration / hardware address = 0000
0	0x134A	from EEPROM / Table 9 (EEP)	Special function / hardware address adjustable

Table 7: Configuration inputs

PIN	Configuration of	Special functions if EEPROM configuration
CFGTPP<0>/HWA<0>	Minimum edge distance TPP – Bit 0	Hardware address Bit 0
CFGTPP<1>/HWA<1>	Minimum edge distance TPP – Bit 1	Hardware address Bit 1
CFGGAIN<0>/HWA<2>	Nominal amplitude – Bit 0	Hardware address Bit 2
CFGGAIN<1>/HWA<3>	Nominal amplitude – Bit 1	Hardware address Bit 3
CFGMODE<0>/Teach	ABZ mode – Bit 0	Trigger pulse for counter value storage
CFGMODE<1>/Zero	ABZ mode – Bit 1	Trigger pulse for counter value reset
CFGDH/TRG	Digital hysteresis – Bit 0	Trigger signal

6.2 Configuration

The IC can be connected to various measuring systems and subsequent electronic systems by way of configuration registers. If the IC is initialised using an EEPROM or the serial interface (SPI/BiSS), full configuration options are available. In case of initialisation by configuration pins, the most important parameters can be set externally. Table 8 below provides an overview of the configuration possibilities for the GC-IP201(B). Further tables 9 and 10 specify the factory configuration.

Table 8: Configuration options

Parameter	Possible Values	Register / Bit
Interpolation rate	256, 200, 160, 128, 100, 80, 64, 50, 40, 32, 25, 20	CFG1 / IR(3:0)
Minimum edge distance t_{pp}	1, 2, 4, 8, 16, 32, 64, 128	CFG1 / TPP(2:0)
Reference signal processing	Enable, disable, delayed Index 1 period / 1 increment Position 0°-360°, step width 11.25° Modus reset, trigger, adjustment, distance coded	CFG3 / DISZ, ZDEL CFG1 / Z4 CFG3 / ZPOS CFG3 / ZMODE
Signal amplitude nominal	660 mV_{pp}, 330 mV_{pp}, 160 mV_{pp}, 50 mV_{pp}	CFG1 / GAIN(1:0)
Analog low-pass Filter	10 kHz, 75 kHz, 200 kHz, 450 kHz, inactive	CFG2 / LP(1:0), DISLP
Digital Hysteresis	0 (disable), 1 … 7	CFG1 / DHE(2:0)
Output Signals A/B/Z	ABZ, DSP-Mode, sensor- and reference point adjusting	CFG1 / MODE (2:0)
Error processing	Masking, latch enable, behaviour of ABZ-output in case of error	CFG1 / Mxxx, Lxxx CFG1 / HLD,TRI
Phase correction	± 10° step width 1.4°, ±5° step width 0.7°	CFG2 / PHBER, PH(2:0)
Low-pass filter	Enable, Disable	CFG1 / LPF
Amplifier control	Pre-setting / time constant / enable, disable	CNTRLG, CFG2 / GAINCTL, DISCTL
Offset control	Pre-setting / time constant / enable, disable	CNTRLO, CFG2 / OFFSCTL, DISCTL
Hardware address	0-15	CMD / SETHWA
Special function	Trigger edge Teach active / inactive Measuring timer Counter zero position (Preset)	CFG1 / TRGSLP CFG1 / TEAN CFG2 / VT(1:0),T(7:0) PRE_ST, CFG3 / PRE_MT
Interface configuration	Data format position values SPI mode synchronous, asynchronous SPI timing BiSS active, inactive* SSI timing BiSS timing* BiSS data format 8Bit, 32 Bit*	CFGBISS / SSI13, MTBIT, GRAY, STBIT CFG2 / ASYNC, SYNC(4:0) CFG3 / SPISLOW CFG3 / SSI CFGBISS / SSITO, CLK10, RING CFGBISS / BISSTO, CLK10 CFGBISS / READ32

* GC-IP201B only

A detailed description of all configuration bits is shown in chapter 9

Table 9: Default configuration

Configuration	Default (EEPROM with factory setting)		Default (Pin)	
Analog	Phase correction Low pass -1dB Nominal amplitude	0° 450 kHz **660 mVpp**	Phase correction Low pass -1dB Nominal amplitude	0° 450 kHz **configurable via Pin**
Interpolation	Interpolation rate Control Start value Control Reference point	256 active, slow Mean values at 45°	Interpolation rate Control Start value Control Reference point	256 active, slow Mean values at 45°
ABZ output	Mode TPP Digital hysteresis Z Error case	**ABZ** **0** **1** active, 1 increment Hold	Mode TPP Digital hysteresis Z Error case	**configurable via Pin** **configurable via Pin: 0...3** **configurable via Pin: 0/1** active, 1 increment Hold
Error processing	Monitoring Storage	All errors (ABZ-mode) **active**	Monitoring Storage	All errors (ABZ-mode) **inactive**
Special functions	Zero Teach Preset values	**active** **inactive via CFG1/TEAEN** 0x00	Zero Teach Preset values	**always inactive** **always inactive** 0x00

Table 10: Default configuration interfaces

Configuration	Default (EEPROM with factory setting)		Default (Pin)	
SPI interface	Activatable via SEN **Hardware address at `CFGGAIN/CFGTPP`** Mode	slow	Activatable via SEN **Hardware address 0000** Mode	slow
SSI interface	GC-IP201 Activatable via SEN	GC-IP201B inactive	GC-IP201 Activatable via SEN	GC-IP201B inactive
	Time out Format	20 µs @ 40 MHz, Ring mode 13Bit Single turn	Time out Format	20 µs @ 40 MHz, Ring mode 13Bit Single turn
BiSS interface	GC-IP201 inactive	GC-IP201B Activatable via SEN	GC-IP201 inactive	GC-IP201B Activatable via SEN
	Hardware address at `CFGGAIN/CFGTPP` Time out Format	 25.6 µs @ 40MHz 30Bit Single turn	**Hardware address 0000** Time out Format	 25.6 µs @ 40 MHz 30Bit Single turn

7 Description of Functions

7.1 Input amplifier / Low pass filter

The GC-IP201 / GC-IP201(B) incorporates three instrument amplifiers with adjustable gain factors. Incremental encoders with a voltage interface and measuring bridges can be connected directly. Sensors with current interface are adapted by way of a simple external circuit (see also 11.1) The IC operates with both single-ended and differential input signals. The amplification is identical for all signals of the sensor (sinusoidal, cosinusoidal, index/reference). To adapt the GC-IP201 / GC-IP201(B) to customised sensors, the mean voltage of the instrument amplifier is provided at pin V0. The instrumentation amplifiers are connected to the internal AD-converters. The connection to the ADC can be directly or via a configurable low pass filter (see also table 12). The voltage level at the ADC inputs can be monitored at the special outputs SMON and CMON.

Table 11: Configuration nominal amplitude (Register CFG1)

CFG1/GAIN(1:0)	00	01	10	11
Input voltage for differential supply[1)] (mV_{pp})	330	165	80	25
Input voltage $U_{DiffNom}$ nominal (mV_{pp})	**660**	**330**	**160**	**50**
Input voltage range for U_{Diff} (mV_{pp})	400...800	200...400	100...200	30...60
Input voltage range to ADC overflow $U_{DiffMAX}$ (mV_{pp})	990	495	240	75
Mean voltage at V0 nominal	1.1	1.1	1.1	1.1
Output voltage U_{MON} nominal at SMON / CMON (V_{pp})	1.27	1.27	1.27	1.27
Gain factor (U_{MON} / U_{DIFF})	1.92	3.85	7.94	25.4

[1)] at each of the inputs SINP, SINN, COSP, COSN

Table 12: Configuration Low pass filter (Register CFG2)

Cut of frequency -1dB	CFG2/DISLP	CFG2/LP(1:0)
450 kHz	0	00
200 kHz	0	01
75 kHz	0	10
10 kHz	0	11
Low pass filter inactive	1	any

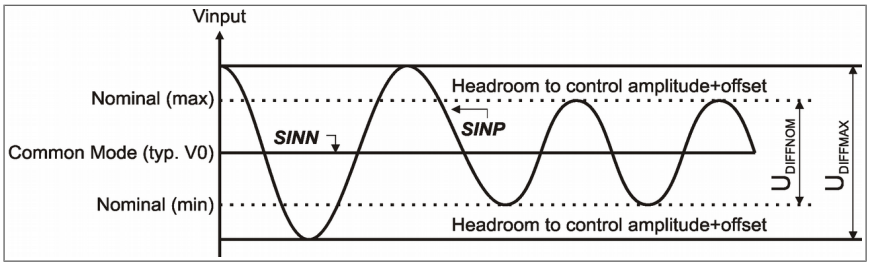


Figure 3: Input signals (single-ended)

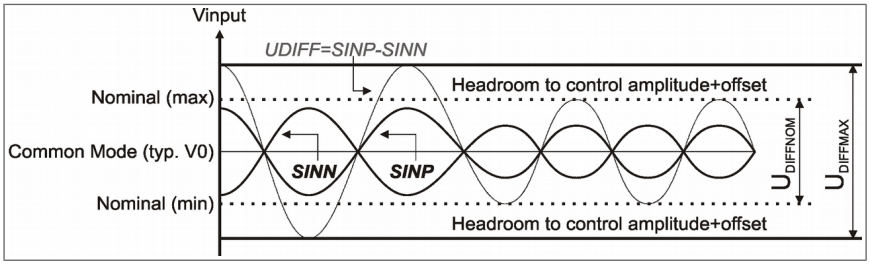


Figure 4: Input signals (differential)

The inputs of the instrumentation amplifiers have an input level limitation of Vin=0.35 V…VDDA-1.00 V. Therefore, the operation area for the gain setting “00” (V_{NOM} = 660 mV_{pp}) is limited by the common mode voltage at the analog inputs.

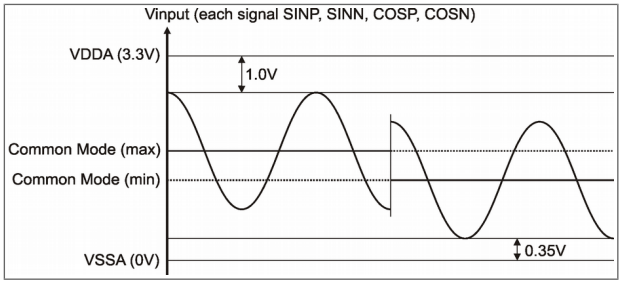


Figure 5: CMIR (input signals)

The following table shows some possible combinations of common-mode voltage and VDDA in case of maximum amplitude for single-ended signals (800 mV_{pp}) and maximum offset (±70 mV) exemplary:

Table 13: Example Common mode input voltage (CMIR)

VDDA	Common mode voltage (Min)	Common mode voltage (Max)
3.30V	0.82V	1.83V
3.15V	0.82V	1.63V
3.00V	0.82V	1.53V

7.2 Signal correction

The input signals are subjected to an AMAC-specific internal gain and offset control. The amplitudes are controlled in the range between 60 % and 120 % of the standard amplitude. The control range for the offset of the two input signals is ±15 % of the nominal amplitude. The phase displacement of the input signals can be corrected statically in 16 steps using a digital potentiometer. The setting range of the phase is set to approx. ±5° or approx. ±10° by way of a configuration bit. After resetting of the IC, start values to correct amplitude and offset of the two input signals are loaded from the EEPROM.
The full measuring accuracy of the IC, however, is only achieved after settling of the internal signal control and after approximately 10 to 50 signal periods.
To achieve the maximum possible accuracy in the amplitude and offset control, the phase potentiometer must be matched with the sensor connected to the GC-IP201(B). Amplitude and offset errors are treated as a unit in the GC-IP201(B). This means that for particular applications a larger permissible error may be permitted for the respectively other parameter under certain circumstances. The attenuation of the controlled system implemented in the GC-IP201 (B) can be adjusted (Register `CFG2/GAINCTL` and `CFG2/OFFSCTL`).

Table 14: Signal correction

Parameter	*as a percentage referred to the nominal amplitude (PEAK-PEAK)*	as a percentage referred to the ADC maximum (PEAK-PEAK)	in mV referred to the standard signal ($1V_{pp}$)	in V on the pin SMON or CMON (PEAK-PEAK)
Maximal value at the input ($Vmax_{pp}$)	150	100	990	1.90
Nominal value of the input signal ($Vnom_{pp}$)	100	66.7	660	1.27
Guaranteed control range for the amplitude	60 ... 120	40 ... 80	400 ... 800	0.76 … 1.52
Setting range of the amplitude controller	56 ... 168 [1)]	37 ... 112 [1)]	370 ... 1110 [1)]	0.71 … 2.13 [1)]
Vector monitoring[2)]	30	20	200	0.38
Guaranteed control range for the offset (Sensor)	±15	±10	±100	±0.191
Setting range of the offset controller	±25	±17	±165	±0.315

[1)] The setting range for the amplitude is greater than the control range of the ADC. Therefore, the upper limit of the setting range cannot be fully utilised for the analog signals.
[2)] An aggregate signal from sine and cosine is monitored. See also chapter 7.5 Bit VLOW

7.3 Interpolation

The signal periods of the analog sinusoidal (SIN) and cosinusoidal input signals (COS) are divided according to the selected interpolation rate and are provided as phase value (PHI) and as a count value to the serial interfaces (SPI/SSI/BiSS). At the same time, square-wave sequences with 90° phase shift (A/B/Z signals) are generated. Furthermore the number of detected references marks are count signed. For rotary encoder application a multi-turn counter is integrated.

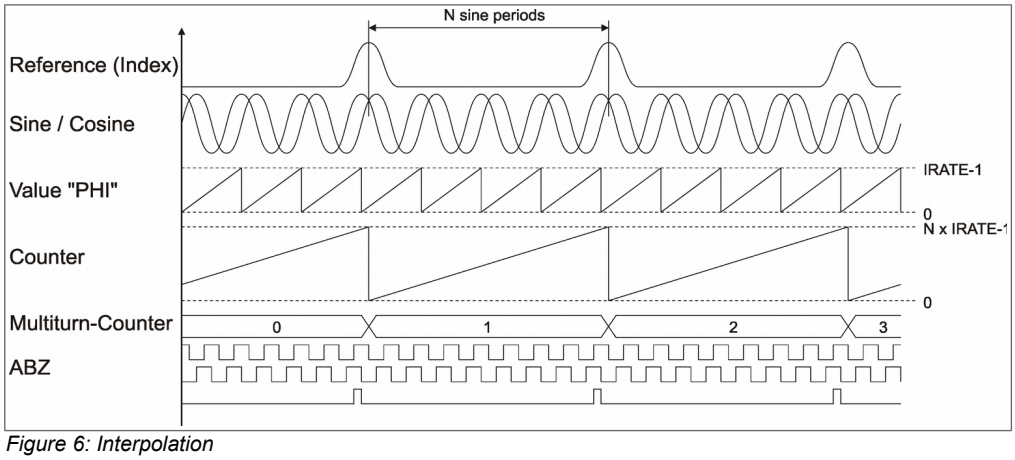


Figure 6: Interpolation

7.3.1 Interpolation rate

Possible interpolation rates (IRATE) which can be selected are 256, 200, 160, 128, 100, 80, 64, 50, 40, 32, 25 or 20. The term 'interpolation rate' is here understood as the number of increments into which the sinusoidal / cosinusoidal period of the input signals is divided. This corresponds to the number of signal transitions at the A/B outputs per input signal period. The number of square-wave periods at the outputs A and B amounts to ¼ of the interpolation rate.

ⓘ *Please note that the interpolation rates 50 and 25 may not be chosen in case of processing of the ABZ signals. If the internal counter is used the interpolation rates can be used.*

7.3.2 Edge distance control / Interval time t_{pp} / Hysteresis

The output signals A,B and Z will change within the time distance t_{pp}, which can be set to a minimum value via the configuration bit CFG1/TPP(2:0) in binary steps. After switching of one of the outputs, the subsequent edge of the other signal will only be visible at the IC output after the time t_{pp} has elapsed. Thus, in case of a short-time disturbance of the input signals, a subsequent interpolation counter will operate without errors. The configuration of edge interval t_{pp} depends on the counter connected to A, B and Z. (see chapter 7.4)
It need to be note that there is a time discretisation at the IC output. Inside the GC-IP201(B) a digital interpolation procedure is implemented. Therefore unpreventable quantisation errors (so called ±1 errors) will interference the speed proportional output signals. Those effects can be reduced by activating the digital hysteresis function (Register CFG1/DH(2:0). This prevents switching of the outputs with static input signals. In this case, all output signals are delayed by the selected hysteresis value.

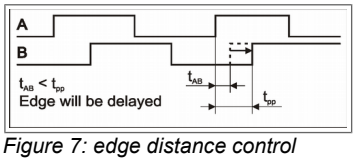
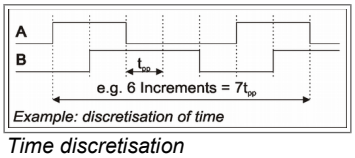
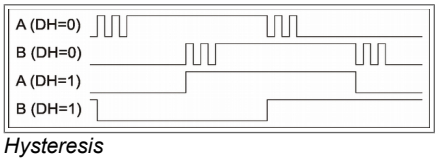


Figure 7: edge distance control



Time discretisation



Hysteresis

7.3.3 Index signal Z

The zero signal Z is generated when the differential voltage of the reference inputs REFP and REFN is positive and the sinusoidal and cosinusoidal analog signals exceeds the phase angle value which is stored in the Register CFG3 (bit ZPOS(4:0). That angle is set to 45 degrees as default setting. The width of the zero signal Z (reference pulse) at the output can be switched between 1 and 4 increments, i.e. between ¼ and 1 period of the output signals A and B. If the IC is configured to the reference width of 1 increment (¼ period), the outputs A and B carry H level with activated Z signal. The phase angle adjustment for reference signal detection can be done using test signals or by a special trigger mode. See also chapter 7.7
The following Figure shows the correlation between the analog input signals, the output signals A,B and Z and the internal counter value .

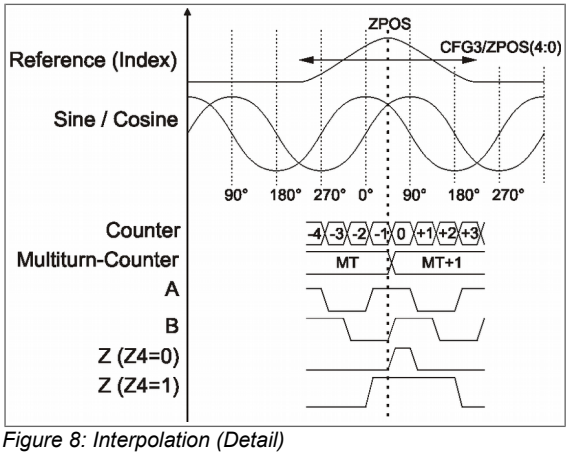


Figure 8: Interpolation (Detail)

7.4 Mode / Maximum input frequency

The maximum input frequency is dependent on the selected interface at the output. If the square-wave sequences (A/B/Z) are used as the output signal, the maximum input frequency is limited by the interpolation rate and by the minimum edge interval (t_{pp}). If exclusively the internal count value is used (interfaces SPI, SSI or BiSS), the maximum input frequency is determined by the clock frequency (f_{OSZ}) . The mode **and** the monitored frequency are switched by way of the bit MABZ in the register CFG1. If both output interfaces are to be used at the same time, the bit MABZ must be initialised with "1".

Table 15: Maximum input frequency

Mode	CFG1/MABZ	Maximum frequency for counter	Maximum frequency for ABZ output
counter	0	$f_{max\_cnt} \approx f_{OSZ}$ / 90 (with controller disabled) $f_{max\_cnt} \approx f_{OSZ}$ / 96 (with controller enabled)	No error detection
square wave, $t_{pp} = N/f_{OSZ}$ $N = 2^{CFG1\text{-}TPP(2:0)}$	1	$f_{max} \approx 0.9 \cdot f_{OSZ} / IRATE < f_{max\_cnt}$	$f_{max} \approx 0.90 \cdot f_{OSZ} / (N \cdot IRATE) < f_{max\_cnt}$ (if N=1) $f_{max} \approx 0.95 \cdot f_{OSZ} / (N \cdot IRATE) < f_{max\_cnt}$ (if N>1)

The limit values obtained are a maximum input frequency of 440 kHz at a clock frequency of f_{OSZ} = 40MHz and a guaranteed edge interval of 32µs at a minimum clock frequency of f_{OSZ} = 4MHz. The GC-IP201(B) can be matched to the subsequent electronics in the range between these two values by appropriate selection of clock frequency and edge interval. All values are valid with matched phase between the input signals and after the settling of the internal signal control. The input frequency up to this time may only amount to 50 % of the specified maximum frequency.

ⓘ *Enabling the internal signal controller reduces the maximum input frequency to f_{OSZ}/96.*
ⓘ *In case of an activated low pass filter either the maximum frequency of input signals will be limited. See also chapter 7.1.*

7.5 Sensor monitoring

The interpolation ICs GC-IP201(B) provides 9 sources for generation of an error signal by monitoring the quality of the sensor signals and errors at the analog input signals. Each source can be activated, deactivated or saved using the relevant bit in the register CFG1. The OR combination of the error signals saved or masked in this way is provided at the pin NERR (L-active). Via the serial interfaces the error flags as well as combined error or warning information can be read out. In case of error, the behaviour of the outputs A, B and Z is not defined. If the HLD bit is set in the register CFG1, the outputs will not change in case of error. If the TRI bit is set in the register CFG1, the outputs will high Z in case of error. A further processing unit can detect that mode as an error.

ⓘ *If the error signal NERR has been activated or one of the error bits has been set in the result register, the current measurement result and all subsequent results must be discarded. After rectification of the error cause and resetting of the error bits (SPI command: RESCNT or via the ZERO-signal), it is imperative to pass through the reference point to be able to perform further absolute measurements.*

Table 16: Overview sensor monitoring

Name	Meaning	SPI	ABZ / SSI	BiSS
EVLOW	Signal vector from Cosine and Sine is too small	Status bit	Error	Error
EADC	One or both A/D converters are overdriven.	Status bit	Error	Error
EOFFS	The offset controller has reached its limit.	Status bit	Error	Warning
EGAIN	The gain controller has reached its limit.	Status bit	Error	Warning
EFAST	Input frequency too high	Status bit	Error	Error
EABZ	The signals A, B and Z are invalid.	Status bit	Error	-

The suggested sensor monitoring configuration is dependent on the used interfaces and can be configured by the user in the register CFG1. It is recommended to activate all monitoring sources. For IC operation without ABZ use the frequency monitoring function (bit MABZ) can be deactivated. See also chapter 7.4.

Table 17: Recommended configuration sensor monitoring

	ABZ-Interface	SPI-Interface	SSI-Interface	BiSS-Interface
Active monitoring bits	EVLOW EADC EOFFS EGAIN EFAST **EABZ**	EVLOW EADC EOFFS EGAIN EFAST	EVLOW EADC EOFFS EGAIN EFAST	EVLOW EADC EOFFS EGAIN EFAST
Monitoring bit evaluation	As total error within the error signal NERR	Status register Position register Error signal NERR	As total error within the data stream	As 2 Bit total error and warning within the data stream
Storage of the monitoring bits	Deactivate	Activate	Activate	Activate
Delete error storage	-	Command RESCNT ZERO-signal	ZERO-signal	Command RESCNT ZERO-Signal
ABZ behaviour in error case	Hold and/or Tristate	any	any	any
Register CFG1(31:16)	0x007F	0x3777	0x3777	0x3777

7.5.1 Error sources

Following the monitored sensor signal parameters are described more detailed. The correspondent bits are displayed in the registers CFG1 and STAT.

Vector error

The signal vector generated from the sinusoidal and cosinusoidal signals is smaller than 30% of the nominal amplitude. Usually, the cause is a partly or completely disconnected sensor. Another cause are input signals with very large offset at simultaneously low amplitude.

Activation error detection	Activation error storage	STAT register	BiSS-SCD	SSI-DATA
Bit MVLOW	Bit LVLOW	Bit EVLOW	Bit1 – Error (L-active)	Bit0 – Error (H-active)

ADC error

One or both A/D converters are overdriven. The cause is that the signal amplitude is too high. Another cause are input signals with very large offset at simultaneously high amplitude. If appropriate pull-up or pull-down resistors are connected to the signal inputs, partly or fully disconnected sensors can also be detected by way of this error bit.

Activation error detection	Activation error storage	STAT register	BiSS-SCD	SSI-DATA
Bit MADC	Bit LADC	Bit ESADC (Sine) Bit ECADC (Cosine)	Bit1 – Error (L-active)	Bit0 – Error (H-active)

Offset error

The offset controller has reached its limit. The cause is an excessive signal offset, a partly or fully disconnected sensor or an invalid value for initialisation of the offset controller.

Activation error detection	Activation error storage	STAT register	BiSS-SCD	SSI-DATA
Bit MOFF	Bit LOFF	Bit ESOFF (Sine) Bit ECOFF (Cosine)	Bit0 – warning (L-active)	Bit0 – Error (H-active)

Amplification error

The gain controller has reached its limit. The cause is either that the signal amplitude is too low or the sensor is partly or fully disconnected.

Activation error detection	Activation error storage	STAT register	BiSS-SCD	SSI-DATA
Bit MGAIN	Bit LGAIN	Bit ESGAIN (Sine) Bit ECGAIN (Cosine)	Bit0 – warning (L-active)	Bit0 – Error (H-active)

Speed error

The input frequency is so high that no A/B signals can be generated or the direction can no longer be detected. The monitored frequency is different depending on whether an internal counter or the square-wave outputs A/B/Z are used. See chapter Fehler: Referenz nicht gefunden.

Activation error detection	Activation error storage	STAT register	BiSS-SCD	SSI-DATA
Bit MFAST	Bit LFAST	Bit EFAST	Bit1 – Error (L-active)	Bit0 – Error (H-active)

ABZ Error

The signals A, B and Z are invalid. The cause is an excessive input frequency. The monitored frequency depends on the set minimum edge interval t_{pp}. This error bit will also be set, if the interpolation rate or the minimum edge interval t_{pp} is changed. Detection of this error has to be deactivated for using the GC-IP201(B) with internal counter only (MABZ = 0).

Activation error detection	Activation error storage	STAT register	BiSS-SCD	SSI-DATA
Bit MABZ	Bit LABZ	Bit EABZ	-	Bit0 – Error (H-active)

7.6 Outputs ABZ

The meaning of the signals at the pins A, B and Z can be modified via the bits MODE(2:0) in the register CFG1. By default, the standard square-wave sequences offset by 90° are generated. If the internal counter of the IC is used, the mode "Controller/DSP" can be activated. Thus, it is possible to carry out equidistant measurements, to synchronise additional components with the IC and to transfer measured values to a controller IC controlled by way of interrupts. Three further modes provide test signals for the sensor adjustment at the outputs A, B and Z.

Table 18: ABZ modes (Register CFG1)

Mode	Use	Mode(2:0)	Output A	Output B	Output Z
Standard	Standard ABZ	000	Square wave A	Square wave B	Index signal Z
Sensor adjust 1	Sensor adjust	001	Test signal IR4C	Test signal IR4S	Reference comparator REFCOMP
Sensor adjust 2	Sensor adjust	010	Test signal IR8C	Test signal IR16C	Control deviation NDEV
Sensor adjust Z	Reference position adjusting	011	Reference (synchronous) REF_SYNC	Counter index point ZCNT	Index signal Z
MC/DSP	Counter to an microcontroller	100	Timer- /Trigger-Interrupt nINT	Synchronous signal StartSample	Counter index point ZCNT

7.6.1 Standard ABZ

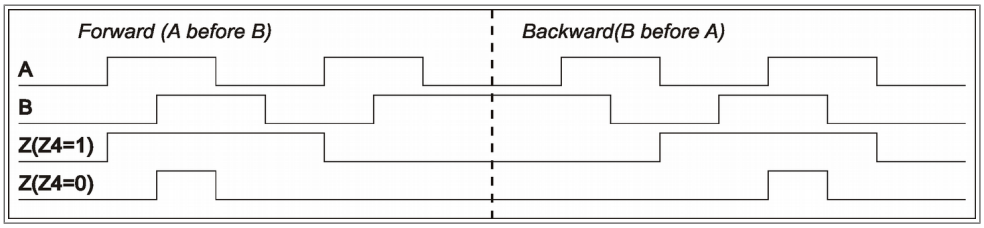


Figure 9: ABZ signals

7.6.2 Controller / DSP

If the measured values of the GC-IP201 (B) are transferred exclusively via the serial interface (SPI/BiSS/SSI), additional signals can be provided at the pins A, B and Z. The pin NERR maintains its meaning. It is designed as an open-drain pin so that the error signals of several ICs can be connected to each other.

Table 19: DSP mode

Pin	Signal	Description
A	nINT	Interrupt; L-active; an active signal indicates that at least one of the trigger holding registers is occupied. A read access to the register MVAL provides the 'oldest' measured value saved in the registers. The interrupt can be triggered either by the timer or by a signal at the pin TRG. See chapter 7.7
B	StartSample	Synchronous signal; this signal delivers the sampling time of the integrated ADC. It can be used to synchronise further systems.
Z	ZCNT	Counter zero signal; this signal indicates that the internal counter of the GC-IP201(B) is reset at the reference point (index point).

7.6.3 Reference point position adjustment

The phase angle for reference signal detection can be shift sensor specific via the configuration bits CFG3/ZPOS(4:0). (See Figure 8). Therefore it is possible to measure special additional signals at A, B and Z. Additionally, the measurement value trigger can be used for adjusting the reference position. For this purpose, the configuration the bits CFG3/ZMODE(1:0) need to be initialised with the value „01“. The values TRGVAL1 and TRGVAL2 (see Figure 10) can be determined exactly by reading out the MVAL register. Referring to the interpolation rate, this enables calculation of the reference signal width as well as the position of the processed index signal in regard to the analog reference signal and to the sine signal of the sensor.

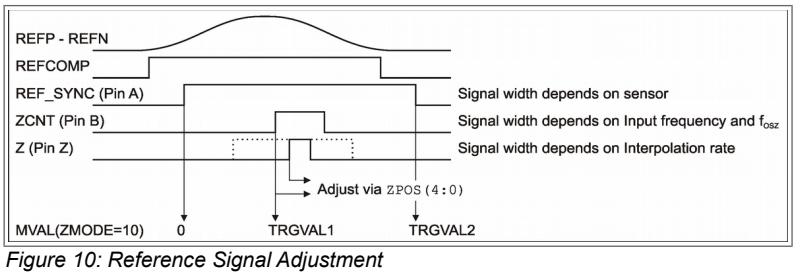


Figure 10: Reference Signal Adjustment

Reference signal width: Zwidth = TRGVAL2/IRATE·360°
Reference signal position: Zstart = Adjusting value ZPOS·11.25° - TRGVAL1/IRATE·360°
Adjustment target: TRGVAL1 = TRGVAL2/2
New Adjustment value: ZPOS_new = (Zstart + Zwidth/2)/11.25°

ⓘ The software for evaluation of *TRGVAL1 and TRGVAL2 should be able to detect if there is no index signal at the output (Z) or that the values in TRGVAL1 or TRGVAL2 are implausible in case of double index signals or if the signals switch between different values. It is recommended to run the sensor adjustment procedure with a smaller signal frequency than the oscillator frequency.*

7.6.4 Sensor adjustment

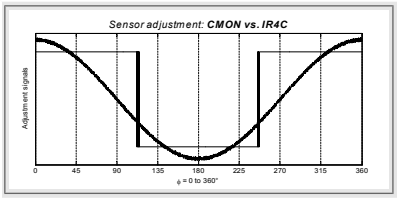
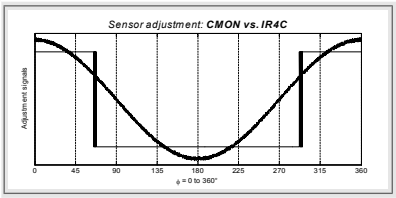
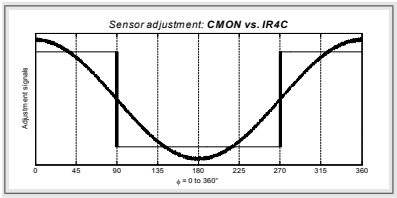
The interpolation ICs GC-IP201(B) contain an automatic gain and offset regulation of the sensor signals. For using the full control range for dynamic errors, statically errors should be adjusted beforehand. Therefore, the output signals at A, B and Z can be used for the fine adjustment in the modes “sensor adjust 1” and “sensor adjust 2”. The output signals of the instrument amplifier are visible at the pins SMON and CMON. A description of the adjustment procedure is shown in table 20. The following figures show typical signal traces.

Table 20: Sensor adjustment

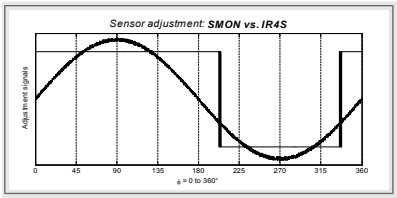
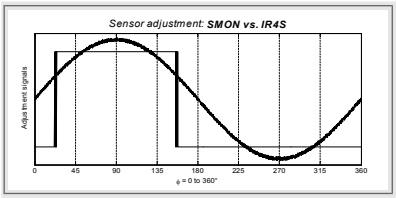
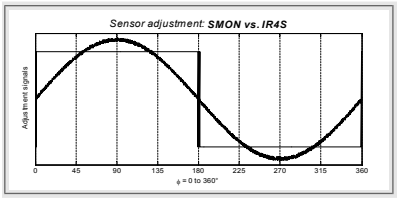
No.	Adjustment	Setting Register CFG1 / CFG2	Setting Procedure
1	Amplitude Sine /Cosine	Gain factor adjustment	Moving the sensor, voltage measuring at the pins SMON and CMON Adjustment until both amplitudes shows 1.27V_{pp}.
2	Reference	Mode: „Sensor adjust 1“	Measuring the signal REFCOMP; Adjustment until the signal width equates approximately one period of the sine signal
3	Offset Cosine	Modus: „Sensor adjust 1“ Deactivating control (bit DISCTRL = 1). Correction values in the centre of the adjusting range	Moving the sensor, voltage measuring at the pins CMON and signal IR4C. Adjustment until the duty cycle at IR4C is approximately 50% of the period at CMON.
4	Offset Sine	Modus:„Sensor adjust 1“ Deactivating control (bit DISCTRL = 1). Correction values in the centre of the adjusting range	Moving the sensor, voltage measuring at the pins SMON and signal IR4S. Adjustment until the duty cycle at IR4S is approximately 50% of the period at SMON.
5	Phase (coarse)	Modus: „Sensor adjust 2“ Activating control (Bit DISCTRL = 0).	Moving the sensor, voltage measuring at the pins CMON and signal IR16C. Coarse phase adjustment until all edges at IR16C are evenly spread within the sine period.
5	Phase (fine)	Modus: „Sensor adjust 2“ Activating control (Bit DISCTRL = 0).	Moving the sensor, voltage measuring at the pins CMON and signal NDEV. Phase adjustment until there is no correlation between the frequency at NDEV and the sine frequency.
6	Amplitude equality	Modus:„Sensor adjust 2“ Deactivating control (bit DISCTRL = 1). Correction values in the centre of the adjusting range	Moving the sensor, voltage measuring at the pins CMON and signal IR8C. Coarse phase adjustment until all edges at IR8C are evenly spread within the sine period.

Table 21: Sensor adjustment

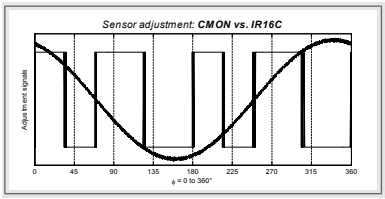
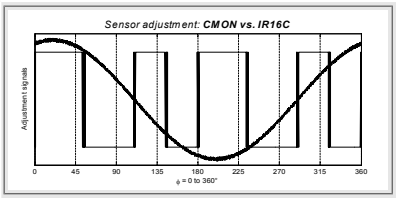
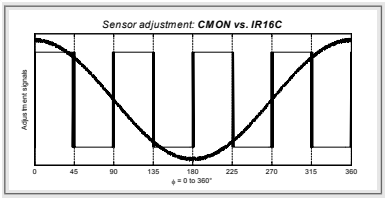
Offset adjusting cosine – signals CMON and IR4C (output A)
Mode '001' (Sensor adjust 1), Control inactive / Correction value: mean value of the correction range

Offset Cosine **positive** Duty cycle IR4C > 50%	Offset Cosine **negative** Duty cycle IR4C < 50%	Offset Cosine **adjusted** Duty cycle IR4C = 50%
		

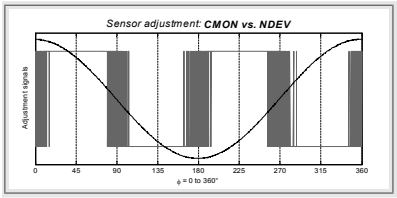
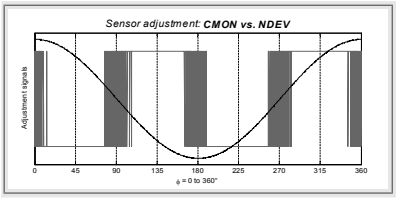
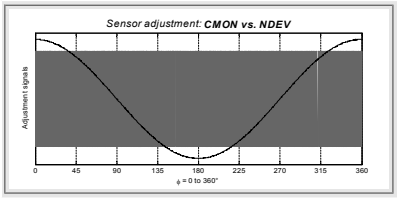
Offset adjusting sine – signals SMON and IR4S (output B)
Mode '001' (Sensor adjust 1), Control inactive / Correction value: mean value of the correction range

Offset sine **positive** Duty cycle IR4S > 50%	Offset sine **negative** Duty cycle IR4S < 50%	Offset Sine **adjusted** Duty cycle IR4S = 50%
		

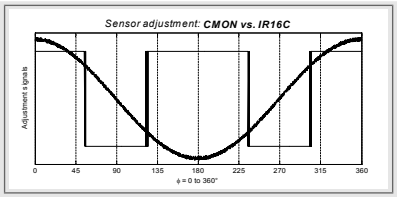
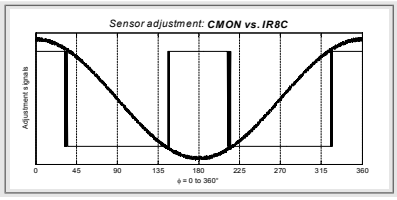
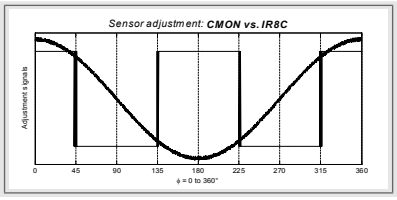
Phase adjusting (coarse) – signals CMON and IR16C (output B)
Mode '010' (Sensor adjust 2), Control active

Phase between cosine and sine **> 90°** Duty cycle IR16C ≠ 50% H-L-edge IR16C at φ < 45°	Phase between cosine and sine **< 90°** Duty cycle IR16C ≠ 50% H-L-edge IR16C at φ > 45°	Phase between cosine and sine **adjusted** Duty cycle IR16C = 50% H-L-edge IR16C at φ = 45°
		

Phase adjusting (fine) – signals CMON and NDEV (output Z)
Mode '010' (Sensor adjust 2), Control active

Phase between cosine and sine **>≈ 90°** Frequency (NDEV) ≈ ½·Frequency(CMON) H-level NDEV at φ = 45°	Phase between cosine and sine **<≈ 90°** Frequency (NDEV) ≈ ½·Frequency(CMON) L-Level NDEV at φ = 45°	Phase between cosine and sine **adjusted** Frequency (NDEV) >> Frequency(CMON)
		

Adjustment amplitude equaliy – signals CMON and IRC8 (output A)
Mode '010' (Sensor adjust 2), Control inactive / correktion values: mean values of the correction control range

Cosine amplitude larger Sine amplitude Duty cycle IR8C > 50%	Cosine amplitude smaller Sine amplitude Duty cycle IR8C < 50%	Cosine amplitude equal to Sine amplitude Duty cycle IR8C = 50%
		

7.7 Measurement value trigger

The interpolation ICs GC-IP201(B) contain two trigger holding registers. The current count value is written to one of the these registers by a signal edge at pin TRG. The trigger edge (falling or rising) can be set using the bit TRGSLP in the register CFG1. Furthermore, a timer is integrated which can also initiate a triggering at freely programmable intervals. The respectively 'oldest' value from the trigger holding registers is provided when accessing the register MVAL for reading. If no value is saved, the current count is displayed. The trigger holding register is re-enabled after reading. The trigger source of the next value to be read is saved in the status register (STAT). Furthermore, the bit TRGOVL indicates whether a timer or a trigger pulse was lost. In addition, it can be detected from the bit TRG of the register MVAL if the value was generated from a hardware event (timer or trigger pin). The signal nINT on pin A indicates with an L-level whether or not one of the trigger holding registers is occupied (refer to chapter 7.6.2). The program flow for the software evaluation of the registers MVAL and STAT is shown in chapter 11.3.

Table 22: Trigger mode / Reference point modes

Trigger source	Use
TRG input	Trigger event from external components (i.e. measuring probes) Trigger event from a micro controller for equidistant measurement
Timer	Trigger for equidistant measurement
Reference CFG3/ZMODE=„01“	Trigger event from reference or index signal for software evaluation
Reference CFG3/ZMODE=„10“	Trigger event from reference or index signal for reference point position via software
Reference CFG3/ZMODE=„11“	Trigger event from reference or index signal for evaluation of distance coded reference marks.

TRG input

The current counter value is shifted to one of the trigger holding registers by a signal edge at the input TRG. The active trigger edge is set with CFG1/TRGSLP.

Timer

After the internal timer reached its value, the current counter value will be shifted into one of the two trigger holding registers. The time constant of the timer is defined by using the bits CFG2/VT(1:0) and CFG2/T(7:0) and can be set between $2^6/f_{OSZ}$ and $2^{24}/f_{OSZ}$.

Reference trigger

Each appearance of an index pulse starts the shift of the current counter value into one of the both trigger holding registers.

Reference position adjusting

A rising edge at the analog reference signal resets the internal counter value. The detection of the index pulse through the IC at the set phase angle starts the shift of the current counter value into the first trigger holding register. The falling edge at the analog reference signal starts the shift of the current counter value into the second trigger holding register. After these two trigger events, the Bit ZSTAT is set and the further trigger processing is stopped until an approval by one of the SPI/BiSS commands RESCNT or CLRZ (refer to Figure 10 and chapter 7.6.3).

Distance coded reference mark processing

The first index pulse resets the internal counter. The second index pulse starts the shift of the current counter value into the second trigger holding register. After these two trigger events the Bit ZSTAT is set and the further trigger processing is stopped until an approval by one of the SPI/BiSS commands RESCNT or CLRZ. Both index pulses have to differ in at least two input signal periods. The calculation of the sensor's absolute position from the all further counting value will be done by the external processing software (refer to chapter 11.5).

7.8 Measurement value registers POSIT, CNT, MVAL and STAT

The interpolated counter values, the trigger holding values, the position values as well as the sensor monitoring information can be read out from various registers via the serial interfaces.
The following table shows what registers can be used for different applications and interfaces. For the BiSS interface it can be chosen between register data (slow communication) and single-cycle-data (SCD; fast communication). Program flows are described in chapter 11.3 .

Table 23: Position register

	SPI	SSI	BiSS
Register CNT	Interpolation counter 30 Bit Index point state 1 Bit Error state 1 Bit	-	Interpolation counter 30 Bit Index point state 1 Bit Error state 1 Bit
Register MVAL	Interpolation counter 30 Bit Trigger value 30 Bit Error state 1 Bit Trigger state 1 Bit	-	Interpolation counter 30 Bit Trigger value 30 Bit Error state 1 Bit Trigger state 1 Bit
Register POSIT	Interpolation counter 8-30Bit Multi-turn counter 0-16Bit Error state 2 Bit	-	SCD use
Register STAT	Error state 9 Bit Trigger state 4 Bit Index point state 1 Bit	-	Error state 9 Bit Trigger state 4 Bit Index point state 1 Bit
SCD (BiSS) / SSI-Data	-	Interpolation counter 8-24 Bit Multi-turn counter 0-16 Bit Error state 1 Bit	Interpolation counter 8-30 Bit Multi-turn counter 0-16 Bit Error state 2 Bit

The data format of the position data (register `POSIT`) is defined in register `CFGBISS` with the bits `STBIT`, `MTBIT` and `GRAY`. Using the bit `MTBIT(1:0)`, the resolution of the multi turn counter is set to 0, 8, 12 or 16 bits. The remaining bits of the transferred `POSIT`-registers will be filled up with the single-turn counter bits. The configuration bits `STBIT(4:0)` define how many bits (LSB) within the single-turn counter are valid. Invalid MSB will be filled up with '0' . The coding of both counter values can be switch between gray code and binary code using the bit `GRAY`. The data length depends on the chosen interface and the bit `SSI13`.

Table 24: Register CFGBISS - configuration data format position data

SSI13	MTBIT	Position data SSI	Position data BiSS	Position data SPI
0	00	24 Bit Single-turn / 8-24Bit resolution 1 Bit error	32 Bit Single-turn / 8-30Bit resolution 1 Bit error / 1 Bit warning	30 Bit Single-turn / 8-30Bit resolution 1 Bit error / 1 Bit warning
0	01	8 Bit Multi-turn 16 Bit Single-turn / 8-16Bit resolution 1 Bit error	8 Bit Multi-turn 24 Bit Single-turn / 8-24Bit resolution 1 Bit error / 1 Bit warning	8 Bit Multi-turn 22 Bit Single-turn / 8-22Bit resolution 1 Bit error / 1 Bit warning
0	10	12 Bit Multi-turn 12 Bit Single-turn / 8-12Bit resolution 1 Bit error	12 Bit Multi-turn 20 Bit Single-turn / 8-20Bit resolution 1 Bit error / 1 Bit warning	12 Bit Multi-turn 18 Bit Single-turn / 8-18Bit resolution 1 Bit error / 1 Bit warning
0	11	16 Bit Multi-turn 8 Bit Single-turn / 8Bit resolution 1 Bit error	16 Bit Multi-turn 16 Bit Single-turn / 8-16Bit resolution 1 Bit error / 1 Bit warning	16 Bit Multi-turn 14 Bit Single-turn / 8-14Bit resolution 1 Bit error / 1 Bit warning
1	XX	12 Bit Single-turn / 8-12Bit resolution 1 Bit error	32 Bit Single-turn / 8-30Bit resolution 1 Bit error / 1 Bit warning	30 Bit Single-turn / 8-30Bit resolution 1 Bit error / 1 Bit warning

ⓘ *In case of the use of the multi turn counter at the BiSS and SSI interfaces one of the following interpolation rates should be set 256, 128, 64 or 32, as the higher-ranking interface master usually can handle binary resolution only. The number of the used bits will be defined in the register* `CFGBISS` *with the bit* `STBIT(4:0)`.

7.9 Counter preset / SPI commands / control signals

The values in the internal counter as well as in the internal multi-turn counter can be preset. Thus, the GC-IP201(B) contains a preset value holding register. Therefore, an application specific zero position is configurable. In combination with the internal EEPROM, this zero position can also be stored permanently. Special SPI commands and signals for configuration read out and storage as well as for counter and regulation control are implemented additionally.

Table 25: Commands / Control signals

Action	Counter and Reg. PRE_ST	Multiturn counter and Reg. PRE_MT	Control	EEPROM
Reference signal (at REFP/REFN)	Counter-Reset to 0	Counter: Incrementation or decrementation	-	-
Reset / SPI/BiSS command RESIC [1]	PRESET-register is loaded from the EEPROM, then this value is transmitted to the counter		Control values are loaded from the EEPROM	Configuration is read from the EEPROM and written to the register
Reset / SPI/BiSS command RESIC [2]	Counter-reset to 0; PRESET-register is initialised with 0		Reset to centre position	-
SPI/BiSS command RESCNT	PRESET-register is written to the counter		-	-
SPI/BiSS command RESCTL	-	-	Reset to centre position	-
SPI/BiSS command WCFG	PRESET-register is written to the EEPROM; No influence on the counter.		Control values are written to the EEPROM	Configuration is read from the register an written to the EEPROM
Falling edge at Zero-signal [1]	PRESET-register is written to the counter		-	-
Falling edge at Teach-signal [1] if bit CFG1/TEAEN = 1	Counter values is loaded into the PRESET-register, Then the PRESET-register is written into the EEPROM		Control values are written to the EEPROM.	Configuration is read from the register an written to the EEPROM

[1] if EEPROM active, refer to chapter 6.1
[2] if EEPROM inactive, refer to chapter 6.1

Referring to Table 25, the counter can be manipulated by SPI/BiSS directly. If the register PRE_ST or PRE_MT is written first and then the register contents are transferred to the counter using the command RESCNT.

The GC-IP201 contains a debouncing circuit for the signals TEACH and ZERO. The respective function is started at the falling edge of the signal. After that, no signal change can be observed for the selected time $t_{debounce}$. In case of a clock frequency f_{OSZ} of 40MHz, the time $t_{debounce}$ is approximately 2.5ms. The TEACH-signal has to be activated by the configuration bit CFG1/TEAEN.

As counter, controller and the EEPROM are influenced by several sources, the following hints have to be noted:

- ZERO and TEACH are not available, if the configuration by pins is active (CFGPIN = 1)
- The TEACH-signal will be suppressed, if an EEPROM access is active
- The ZERO-signal will be suppressed, if an EEPROM access is active
- The command RESCNT will be suppressed, if an EEPROM access is active
- The command WCFG will be suppressed, if an EEPROM access is active
- Incorrect values can be transferred to the counter, if the ZERO-signal is active whilst the PRE_ST- or PRE_MT-Register is written by SPI/BiSS.
- For the use of the command WCFG and the TEACH signal, the number of maximum EEPROM write cycles has to be considered.

7.10 Signal propagation time

The analog propagation time of the input signal through the instrumentation amplifier of the GC-IP201(B) is defined by the chosen gain and the configured cut of frequency of the noise filter. The following table shows reference values for selected configurations.

Table 26: Propagation time analog (td_{ANA})

Configuration	Min	Typ.	Max
CFG2/DISLP = 1; CFG1/GAIN = 00	70 ns	90 ns	110 ns
CFG2/DISLP = 1; CFG1/GAIN = 11	70 ns	125 ns	180 ns
CFG2/LP(1:0) = 00 (450 kHz)	220 ns	260 ns	350 ns
CFG2/LP(1:0) = 01 (200 kHz)	450 ns	500 ns	580 ns
CFG2/LP(1:0) = 10 (75 kHz)	1.1 us	1.2 us	1.3 us
CFG2/LP(1:0) = 11 (10 kHz)	7.2 us	7.4 us	7.6 us

The propagation time between sampling start and the measurement result in the registers `MVAL`, `POSIT` or `CNT` is 90 system clock cycles. If an external counter is used at the outputs `A`, `B` and `Z` further 32 system clock cycles have to be added.

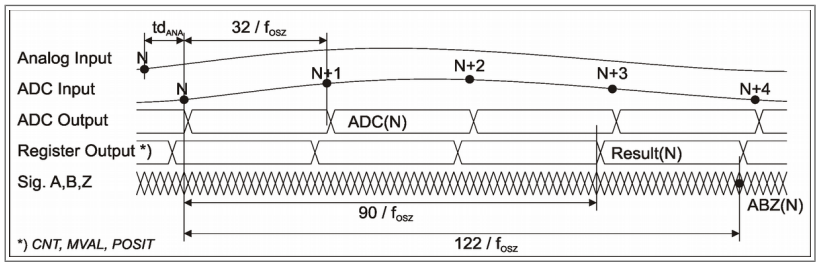


Figure 11: Signal propagation time

ⓘ *Please note that the **constant** propagation delay of the IC (as in every digital system) causes a frequency dependent phase shift between the analog input signals and the output signals. ($\varphi = 2\pi \cdot f \cdot t_d$). The following figures show this behaviour for the output signal Z for two different input frequencies. The behaviour of the square-wave signals A and B is equivalent.*

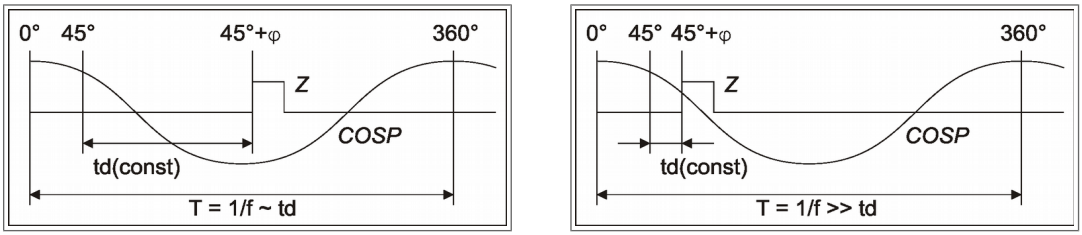


Figure 12: Constant propagation delay

8 Digital Interfaces

8.1 Serial interface SPI

The serial Interface SPI is activated, if the input SEN is on H-level during IC reset procedure. The GC-IP201(B) operates in slave mode. In other words: It cannot start communication itself. Up to sixteen GC-IP201(B) can be controlled on a single interface bus. The interface is compatible to the most important microcontroller families in SPI mode 0 (16 bit data, MSB first, SCK-Default Low, sampling with rising clock edge). It is neither compatible to GC-IP1000B nor to GC-IP200.

8.1.1 Signals

Table 27: SPI signals

Signal	Meaning	Direction
SCK	Clock Clock cycle The data at MOSI is sampled by IC with the rising edge at SCK. The data at MOSI is modified by IC with the falling edge at SCK. The maximum clock frequency depends on the configuration bit CFG3/SPISLOW	IN
SEN	Enable Low: Interface is enabled High: Interface is disabled, MISO becomes high-resistant or is set to nWAIT Rising edge: Command is executed.	IN
MOSI	Master OUT / slave IN Data input	IN
MISO/nWAIT	Master IN / slave OUT Data output and status signal Attention! External pull-up resistor at the pin required!	OUT (Tristate-capable)

During the IC reset procedure and within the waiting ime of a synchronous SPI-read command the MISO line will be held on L-level (meaning of nWAIT).

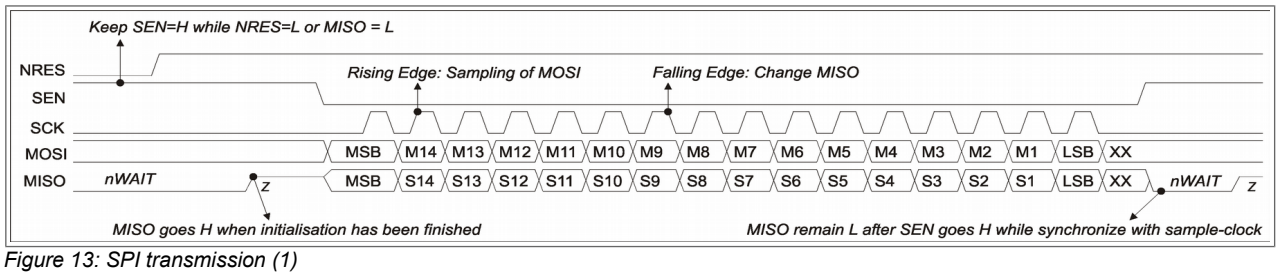


Figure 13: SPI transmission (1)

8.1.2 Protocol

Table 28: SPI protocol

OP-Code	Description	Bit at signal MOSI															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		OPC				HWA				DATA							
WRA	Write address	1	0	0	nB	H3	H2	H1	H0	A7	A6	A5	A4	A3	A2	A1	A0
WRD	Write data	1	0	1	nB	H3	H2	H1	H0	D7	D6	D5	D4	D3	D2	D1	D0
RD0/ST	Read Bytes 0+1 (2 LSB)	1	1	0	X	H3	H2	H1	H0	A7	A6	A5	A4	A3	A2	0	0
RD1	Read Bytes 2+3 (2 MSB)	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X
NOP	Output read register	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

H(3:0): Hardware address, Default: '0000', Will not be evaluated if nB = 0
A(7:0): Register address within an IC
D(7:0): Data word / Write data (read data will appear at MISO)
nB: Broadcast (L-active) 0: command to all IC
1: command to IC which was addressed by H(3:0)

Default-OP-Codes

```
WRA = 0x8000+address        WRD = 0xA000+Data
RD0 = 0xC000+address        RD1 = 0xE000
NOP = 0x0000
```

Any data transfer is initiated by the host processor sending one SPI word. An SPI word consists of a 4 bit OP code, a 4 bit hardware address and up to 8 bits of data. OP codes are only accepted if the hardware address sent corresponds with the hardware address of the GC-IP201(B). The hardware address of the IC after reset is '0000'. The command SETHWA can be used to read the pins HWA<3:0> into the IC as the new hardware address. During the following SPI access, the OP codes for reading out a register result in a output at MISO, independent on the hardware address within the new SPI word.

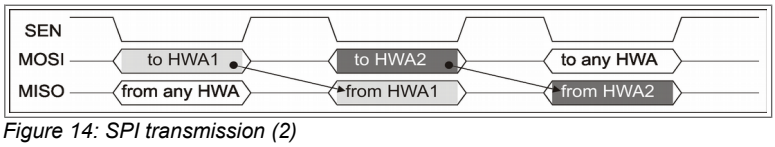


Figure 14: SPI transmission (2)

8.1.3 Register access

The access to the registers within the GC-IP201(B) operates 8 bit reading and 16 bit writing. The registers of these ICs are organised in 32 bit architecture. Data to be read is stored into a 32-bit holding register using the SPI word RD0/ST. The data from the two least significant bytes are output on the pin MISO during the **next** SPI access. The data output of the two MSB at MISO occurs in the SPI-cycle, which follows the SPI word RD1 at MOSI. To read a 32-bit register, the commands RD0/ST, RD1 and NOP are usually executed consecutively. To read multiple registers in succession, the sequence: RD0 – RD1 – RD0 – RD1... can be used.
To write a register, first the register address must be set using the SPI word WRA. Then, the register can be programmed using WRD. 32 bit registers are programmed byte by byte (refer to figure 16).

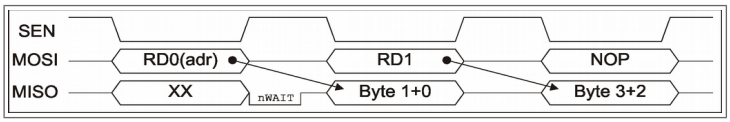
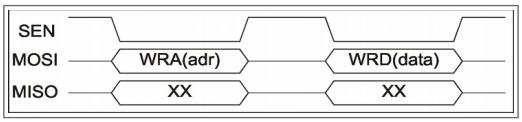


Figure 15: SPI write 8 bit



SPI read 32 bit

Figure 16: SPI write 32 bit

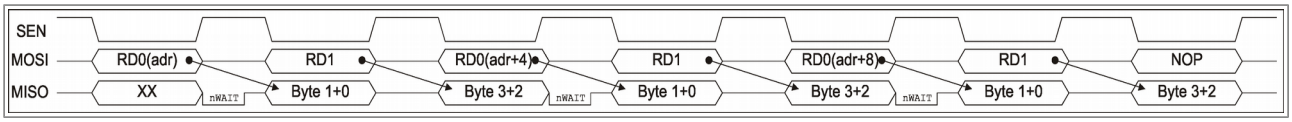


Figure 17: SPI read 3 x 32 bit

8.1.4 SPI – Synchronous / Asynchronous

The 32 bit data is transferred into the holding register synchronously to the internal IC sequence. The value SYNC in the register CFG2 can be used to shift the time relative to the sampling time of the ADC. Thus, it is possible to carry out equidistant measurements with small delays. The pin MISO is low during the waiting time (nWAIT). If the bit ASYNC in the register CFG2 is set, the data is stored immediately after the rising edge at the signal SEN. The time reference to the sampling of the analog signals will be lost. Thus, higher baud rates are achieved. To read the registers MVAL, CNT, POSIT, STAT, CTRLG, CTRLO and ADC any value can be set for SYNC. The default value '00000' provides a small delay between the calculated count value and the data output at the SPI interface. To read the registers PHI, DPHI, BQ and CADC, a value of '00100' must be used.

8.1.5 SPI – Signal filter

Using the configuration bit CFG3/SPISLOW, a digital filter for the SPI input signals SEN,SCK and MOSI can be activated. The maximum SPI clock frequency at SCK is limited to approx. f_{OSZ} / 4.

8.2 BiSS interface

The BiSS interface in Mode BiSS-C of the GC-IP201B is activated in case of L-level at the input SEN and reset of the bit SSI in register CFG3 during the reset procedure. During the IC's initialisation, the levels at the inputs HWA(3:0) are read in as the 4 LSB of the BiSS serial number. Therefore, an connection of numerous ICs at one bus is possible without further programming effort. In order to use the BiSS interface of the GC-IP201B, the EEPROM has to have a valid configuration as basic parameters are included in the EEPROM. For the use of this interface, the bits BISSTO, CLK10 and READ32 in register CFGBISS are initialised in the EEPROM by the end user on the basis of system parameters.

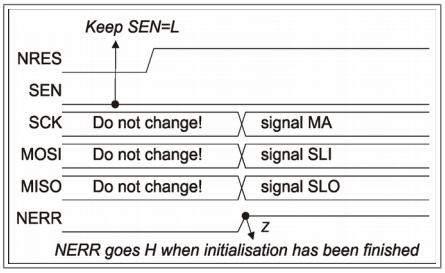


Figure 18: initialisation BiSS hardware

The register POSIT (refer to chapter 7.8) is transmitted in the single-cycle-data of the BiSS protocol with a data length of 40 bits. The data contains the interpolation counter value (=single turn counter) and the multi turn counter value as well as two bit for error information (Error / Warning) and the CRC-check sum (6 bit, inverted). In case of the use of the multi-turn counter, the interpolation rate should be set to the values 256, 128, 64 or 32, as the higher-ranking interface master usually can handle binary resolution only.

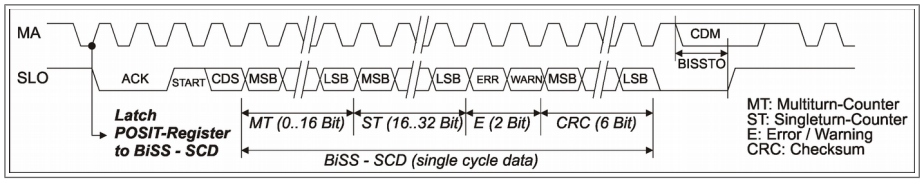


Figure 19: BiSS SCD (Single-Cycle-Daten)

Via access to the BiSS register, all further IC registers are reachable. In case of reading the 32 bit data registers, the bit READ32 in the register CFGBISS has to be set. Register read accesses via BiSS occur in 32 bit format. Always 4 consecutive addressed starting with the least significant one (divisible by 4) are read by the BiSS master. Additionally, the advices for setting the bits SYNC(4:0) in register CFG2 have to be considered as well (refer to chapter 8.1.4).

Table 29: Register CFGBISS (BiSS mode)

Bit	Meaning	Factory configuration	User configuration
BISSTO	BiSS time out	25.6µs bei 40 MHz	BISSTO = $\log_2$(time out·f_{OSZ})
CLK10	Oscillator frequency range	f_{OSZ} > 10MHz	0 for f_{OSZ} ≤ 10MHz / 1 for f_{OSZ} > 10MHz
READ32	Data format read access	Configuration register read	Data and/or configuration register read

Table 30: Presetting BiSS register

Register	Factory configuration	User configuration
BISS serial number	MSB: 0 LSB: level an HWA(3:0)	MSB: unique serial number LSB: level an HWA(3:0)
BISS manufacturer code	0x4743 („GC“)	Own manufacturer code
BISS device code	0x51 0x01 0x1E 0x00 → *11.8*	Own device code
BiSS profile + Electronic data sheet (EDS)	unused	Own device profile

All further descriptions about the BiSS interface, i.e. signal sequences, register descriptions and information regarding the EDS (Electronic data sheet) are available under www.biss-interface.com.

8.3 SSI interface

The SSI interface of the interpolation circuits GC-IP201(B) is activated, if the input SEN has L-level and the bit SSI in register CFG3 is set during the reset procedure. In Order to use the SSI interface of the GC-IP201(B), the EEPROM has to have a valid configuration as basic parameters are included in the EEPROM. The Bits SSITO, CLK10 and RING in register CFGBISS are initialised in the EEPROM by the end user on the basis of system parameters.

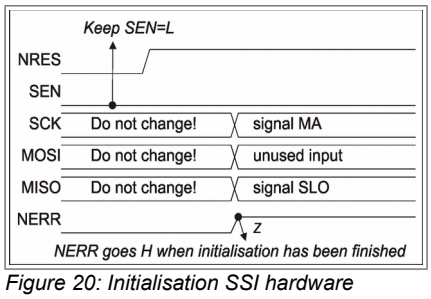


Figure 20: Initialisation SSI hardware

Within the data of the SSI protocol the register POSIT (see also chapter 7.8) is transmitted in a data length of 13 or 25 bits. The data contains the interpolation counter value (= single-turn counter) and the multi-turn counter value. Additionally, a bit for the error information is reserved. If the multi-turn counter is used, the interpolation rate should be set to the value 256, 128, 64 or 32, as the higher-ranking interface master usually can handle binary resolution only. If the bit RING in the register CFGBISS is set, the SSI master is able to enforce a repeatable data transmission of the same value by continuous clock (SSI ring mode).

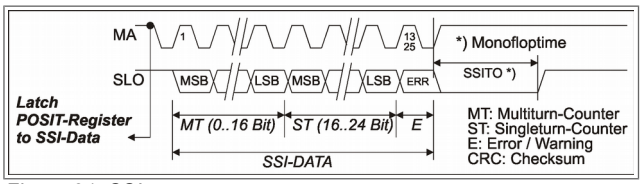


Figure 21: SSI

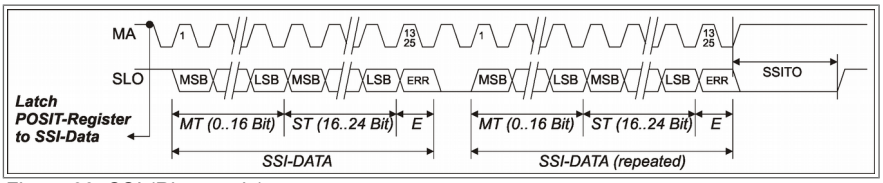


Figure 22: SSI (Ring mode)

Table 31: Register CFGBISS (SSI mode)

Bit	Description	Factory configuration	User configuration
SSITO	SSI time out	20µs at 40 MHz	SSITO = (time out·f_{OSZ})-3
CLK10	Oscillator frequency range	f_{OSZ} > 10MHz	0 for f_{OSZ} ≤ 10MHz / 1 for f_{OSZ} > 10MHz
RING	SSI ring mode	Ring mode	SSI master mode
SSI13	Data length	13 Bit	0 for 25 Bit / 1 for 13 Bit

8.4 EEPROM

For the permanent storage of user specific configuration as well as for all relevant information regarding the BiSS interface, an EEPROM is implemented in the GC-IP201(B). After reset, a test is performed to determine whether the EEPROM is enabled and if the content can be read out. **The EEPROM can be enabled with a stored data word 0x134A at EEPROM address 0x00.** Writing to the EEPROM is always performed via an internal interface which can be accessed via the register `EEP`.
The reading of any EEPROM cells also occurs using that register. Additionally, all necessary information regarding the BiSS operation and electronic data sheet can be read out via the BiSS interface from the EEPROM directly. The addressing and the data format of the EEPROM are different from the addressing of SPI or BiSS.

Table 32: EEPROM addressing

	Register	EEPROM
Data word width	8 Bit	16 Bit
Address word width	8 Bit	8 Bit / EEPROM address = register address / 2
Endianess (user register)	Little Endian	Little Endian
Endianess (BiSS register)	Big Endian	Big Endian

Table 33: Address mapping

Range	Address SPI	Address BiSS	Address EEPROM	Endianess
User register	0x00 … 0x3F	0x00 … 0x3F (Page 0)	0x00 … 0x1F	Little Endian
BiSS-C Slave-Register	-	0x40 … 0x47	0x20 … 0x23	Big Endian
User register	0x48 … 0x77	0x48 … 0x77	0x24 … 0x3B	Little Endian
BiSS-C Slave register	-	0x78 … 0x7F	0x3C … 0x3F	Big Endian
BiSS-C Profile / BiSS-C EDS	-	0x00 … 0x3F (Page 1)	0x40 … 0x5F	Big Endian
BiSS-C Profile / BiSS-C EDS	-	0x00 … 0x3F (Page 2)	0x60 … 0x7F	Big Endian
BiSS-C Profile / BiSS-C EDS	-	0x00 … 0x3F (Page 3)	0x80 … 0x9F	Big Endian
BiSS-C Profile / BiSS-C EDS	-	0x00 … 0x3F (Page 4)	0xA0 … 0xBF	Big Endian
BiSS-C Profile / BiSS-C EDS	-	0x00 … 0x3F (Page 5)	0xC0 … 0xDF	Big Endian
BiSS-C Profile / BiSS-C EDS	-	0x00 … 0x3F (Page 6)	0xE0 … 0xFF	Big Endian

The procedures for EEPROM read out and writing are described in chapter 11.4. It is important to note that in case of a set bit `EEPBSY` bit in the `EEP` register, this register `EEP` may not be written. The configuration bit `CFGBISS/CLK10` has to be set according the clock frequency. The register `MANUFACTURE` may not be changed!

9 Register

Table 34: Register overview

Register	Access [1]	Address SPI	Biss-Page	Address BISS	Address EEPROM [2]	Remarks
MVAL	R	0x00	0	0x00...0x03	0x00...0x01	Validation identifier in EEP
CNT	R	0x04		0x04...0x07		
STAT/ID/REV	R	0x08		0x08...0x0B		
CFG1	RW	0x0C...0x0F		0x0C...0x0F	0x06...0x07	User configuration from EEPROM
CFG2	RW	0x10...0x13		0x10...0x13	0x08...0x09	
CTRLG_C	RW	0x14...0x17		0x14...0x15	0x0A	
CTRLG_S	RW			0x16...0x17	0x0B	
CTRLO_C	RW	0x18...0x1B		0x18...0x19	0x0C	
CTRLO_S	RW			0x1A...0x1B	0x0D	
CFG3	RW	0x1C...0x1F		0x1C...0x1D	0x0E	
PRE_MT	RW			0x1E...0x1F	0x0F	
PRE_ST	RW	0x20...0x23		0x20...0x23	0x10...0x11	
CFGBISS	RW	0x24...0x27		0x24...0x25	0x12...0x13	
POSIT	R	0x28		0x28...0x2B		
ADC_C	R	0x2C		0x2C...0x2D		
ADC_S	R			0x2E...0x2F		
CADC_C	R	0x30		0x30...0x31		
CADC_S	R			0x32...0x33		
IP1_PHI	R	0x34		0x34...0x35		
IP1_DPHI	R			0x36...0x37		
IP2_PHI	R	0x38		0x38...0x39		
IP2_BQ	R			0x3A...0x3B		
MANUFACTURE	!!	0x3C...0x3F		0x3C...0x3F		May not be changed!
BiSS Bank	R (EEP)	-	-	0x40		
BiSS EDS Bank	R (EEP)			0x41	0x20 (MSB)	see www.biss-interface.com
BiSS Profile	R (EEP)			0x42...0x43	0x21	
BiSS- serial number	R (EEP)	-		0x44...0x47	0x22 ... 0x23	4 LSB = HWA
EEP_DAT	RW	0x48...0x4B		0x48...0x49		
EEP_ADR / EEP_STAT	W / R			0x4A		
EEP_OPC	W			0x4B		
unused	-	0x4C..0x4F		0x4C...0x4F		
CMD	W	0x50		0x50		
unused	-	0x51...0x6B		0x51...0x6B		
Manufacture_ZA1	!	0x6C...0x6F		0x6C...0x6F	0x36...0x37	Register and EEPROM cannot be changed
Manufacture_ZA2	!	0x70...0x73		0x70...0x73	0x38...0x39	
Manufacture_ZD	!	0x74...0x77		0x74...0x75	0x3A...0x3B	
BISS device code	R (EEP)	-		0x78...0x7B	0x3C...0x3D	see www.biss-interface.com
BiSS timeout	RW	-		0x7C...0x7D	0x3E	
BiSS manufacturer code	R (EEP)	-		0x7E...0x7F	0x3F	
BISS-EDS	R (EEP)	-	1	0x00...0x3F	0x40...0x5F	
BISS-EDS	R (EEP)	-	2	0x00...0x3F	0x60...0x7F	
BISS-EDS	R (EEP)	-	3	0x00...0x3F	0x80...0x9F	
BISS-EDS	R (EEP)	-	4	0x00...0x3F	0xA0...0xBF	
BISS-EDS	R (EEP)	-	5	0x00...0x3F	0xC0...0xDF	
BISS-EDS	R (EEP)	-	6	0x00...0x3F	0xE0...0xFF	

[1] Legend:

R:	read only (register)
W:	write only (register)
RW:	read/write (register)
R (EEP):	read only via BiSS (EEPROM)
!:	manufacturer register. May or cannot be changed!

[2] The EEPROM Address is valid for reading / writing the EEPROM via the internal internal interface (Register `EEP`) only.

dark grey : Register will be load from EEPROM during Reset (see chapter 6.1)
blue grey : BiSS information, read able form EEPROM directly (see www.biss-interface.com)
white: EEPROM consist validation identifier 0x134A at address 0x00(user) and 0x01(manufacturer)

MVAL — Measurement value / trigger value

31:2	1	0
CNT/TVAL	TRG	ERR

Bit	Name	Reset value	Format	Value	Meaning
31:2	CNT/TRG	0x0000	Signed		Measurement value; value corresponds to count value or contents of a trigger holding register → chapter 7.7
1	TRG	0	Bit	0 1	Measurement value corresponds to current count value Measurement value corresponds to contents of a trigger holding register
0	ERR	0	Bit	0 1	Measurement value is valid An error has occurred. The current measurement value and all subsequent values are to be discarded. After rectification of the error cause and resetting of the error bits (SPI command: RESCNT), it is imperative to pass through the reference point to be able to perform further absolute measurements. → chapter 7.5

CNT — *Count value*

31:2	1	0
CNT	ZSTAT	ERR

Bit	Name	Reset value	Format	value	Meaning
31:2	CNT	0x0000	Signed		Count value
1	ZSTAT	0	Bit	0 1	The reference mark (index) of the scale has not yet been passed or the reference of count value and reference mark was lost due to an error. The reference mark (index) of the scale has been passed; GC-IP201(B) and scale operate synchronously. → chapter 7.3.3, 7.6.3, 7.6.4
0	ERR	0	Bit	0 1	Measured value is valid An error has occurred. The current measured value and all subsequent values are to be discarded. After rectification of the error cause and resetting of the error bits (SPI command: RESCNT), it is imperative to pass through the reference point to be able to perform further absolute measurements. → chapter 7.5

POSIT — *Position data (multi turn + single turn)*

31:2	1	0
POSITION	WARN	ERR

Bit	Name	Reset value	Format	value	Meaning
31:2	Position	0x0000	Unsigned ST Unsigned MT		Position value from multi turn and single turn position Position = MT · INKREMENTS/360°mech. + ST → chapter 7.8
1	WARN	0	Bit	0 1	Measured value is valid Measured value with reduced accuracy → chapter 7.5
0	ERR	0	Bit	0 1	Measured value is valid An error has occurred. The current measured value and all subsequent values are to be discarded. After rectification of the error cause and resetting of the error bits (SPI command: RESCNT), it is imperative to pass through the reference point to be able to perform further absolute measurements. → chapter 7.5

ID / STAT / REV	ASIC identifier / Status

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	ASICID				ASICREV			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	ZSTAT	TRGOVL	TRGZ	TRGTIM	TRGPIN	ESOFF	ECOFF	ESGAIN	ECGAIN	EABZ	EFAST	ESADC	ECADC	EVLOW

Bit	Name	Reset value	Format	Value	Meaning
23:20	ASICID	0101	Binary	0101	The IC is a GC-IP201 or GC-IP201B
19:16	ASICREV	0001	Binary		Silicon revision of the IC
15	-	0	Bit	-	-
14	-	0	Bit	-	-
13	ZSTAT	0	Bit	0 1	The reference mark (index) of the scale has not yet been passed or the reference of count value and reference mark was lost due to an error. The reference mark (index) of the scale has been passed; GC-IP201(B) and scale operate synchronously. → chapter 7.3.3, 7.6.3, 7.6.4
12	TRGOVL	0	Bit	0 1	No overflow of the trigger holding register Overflow of the trigger holding register; Trigger or timer event was lost
11	TRGZ	0	Bit	0 1	Next measured value read at address 0x00 was not triggered by the reference signal Next measured value read at address 0x00 was triggered by the reference signal
10	TRGTIM	0	Bit	0 1	Next measured value read at address 0x00 was not triggered by the timer Next measured value read at address 0x00 was triggered by the timer
9	TRGPIN	0	Bit	0 1	Next measured value read at address 0x00 was not triggered by pin TRG Next measured value read at address 0x00 was triggered by pin TRG
8	ESOFF	0	Bit	0 1	No offset error at sinusoidal signal The offset controller for the sinusoidal signal has reached its limit. The cause is an excessive signal offset, a partly or fully disconnected sensor or an invalid value for initialisation of the controller.
7	ECOFF	0	Bit	0 1	No offset error at cosinusoidal signal The offset controller for the cosinusoidal signal has reached its limit. The cause is an excessive signal offset, a partly or fully disconnected sensor or an invalid value for initialisation of the controller.
6	ESGAIN	0	Bit	0 1	No amplitude error at sinusoidal signal The gain controller for the sinusoidal signal has reached its limit. The cause is either that the signal amplitude is too low or the sensor is partly or fully disconnected.
5	ECGAIN	0	Bit	0 1	No amplitude error at cosinusoidal signal The gain controller for the cosinusoidal signal has reached its limit. The cause is either that the signal amplitude is too low or the sensor is partly or fully disconnected.
4	EABZ	0	Bit	0 1	No error at A/B/Z The signals A, B and Z are invalid. The cause is an excessive input frequency. The monitored frequency depends on the set minimum edge interval t_{pp}. This error also occurs if the interpolation rate or the minimum edge interval is changed. Detection of this error is deactivated for the counter mode.
3	EFAST	0	Bit	0 1	No speed error The input frequency is so high that no A/B signals can be generated or the direction can no longer be detected. The monitored frequency is different depending on whether an internal counter or the square-wave outputs A/B/Z are used.
2	ESADC	0	Bit	0 1	No ADC error at the sinusoidal signal The A/D converter for the sinusoidal signal is overdriven. The cause is that the signal amplitude is too high. This error may also occur with signals with very large offset at simultaneously high amplitude.
1	ECADC	0	Bit	0 1	No ADC error at the cosinusoidal signal The A/D converter for the cosinusoidal signal is overdriven. The cause is that the signal amplitude is too high. This error may also occur with signals with very large offset at simultaneously high amplitude.
0	EVLOW	0	Bit	0 1	No vector error The signal vector generated from the sinusoidal and cosinusoidal signals is too small. Usually, the cause is a partly or completely disconnected sensor. This error may also occur with signals with very large offset at simultaneously low amplitude.

CFG1	Configuration 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TEAEN	TRGSLP	LOFF	LGAIN	LABZ	LFAST	LADC	LVLOW	TRI	HLD	MOFF	MGAIN	MABZ	MFAST	MADC	MVLOW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GAIN1	GAIN0	DH2	DH1	DH0	TPP2	TPP1	TPP0	MODE2	MODE0	MODE1	Z4	IR3	IR2	IR1	IR0

Bit	Name	Reset value	Format	Value	Meaning
31	TEAN	0	Bit	0 1	Teach function inactive Teach function active → chapter 7.9
30	TRGSLP	0	Bit	0 1	A falling edge at pin TRG accepts the measured value into the trigger holding register A rising edge at pin TRG accepts the measured value into the trigger holding register
29	LOFF	0 (Pin) 1 (EEPROM)	Bit	0 1	Detected offset errors (ESOFF/ ECOFF) are not saved. Detected offset errors (ESOFF/ ECOFF) are saved.
28	LGAIN	0 (Pin) 1 (EEPROM)	Bit	0 1	Detected gain errors (ESGAIN/ECGAIN) are not saved. Detected gain errors (ESGAIN/ECGAIN) are saved.
27	LABZ	0 (Pin) 1 (EEPROM)	Bit	0 1	Detected A/B/Z errors (EABZ) are not saved. Detected A/B/Z errors (EABZ) are saved.
26	LFAST	0 (Pin) 1 (EEPROM)	Bit	0 1	Detected speed errors (EFAST) are not saved. Detected speed errors (EFAST) are saved.
25	LADC	0 (Pin) 1 (EEPROM)	Bit	0 1	Detected ADC errors (ESADC/ECADC) are not saved. Detected ADC errors (ESADC/ECADC) are saved.
24	LVLOW	0 (Pin) 1 (EEPROM)	Bit	0 1	Detected vector errors (LVLOW) are not saved. Detected vector errors (LVLOW) are saved.
23	TRI	0	Bit	0 1	The behaviour of the signals A,B and Z is defined by the bit HLD in case of error. The signals A,B and Z are high Z in case of error.
22	HLD	1	Bit	0 1	The behaviour of the signals A,B and Z is not defined in case of error. The signals A,B and Z do not change in case of error; the level is maintained.
21	MOFF	1	Bit	0 1	The detection of offset errors (ESOFF/ ECOFF) is deactivated. The detection of offset errors (ESOFF/ ECOFF) is activated.
20	MGAIN	1	Bit	0 1	The detection of gain errors (ESGAIN/ECGAIN) is deactivated. The detection of gain errors (ESGAIN/ECGAIN) is activated.
19	MABZ	1	Bit	0 1	The detection of A/B/Z errors (EABZ) is deactivated; the IC operates in the counter mode. The detection of A/B/Z errors (EABZ) is activated; the IC operates in the square-wave mode.
18	MFAST	1	Bit	0 1	The detection of speed errors (EFAST) is deactivated. The detection of speed errors (EFAST) is activated.
17	MADC	1	Bit	0 1	The detection of ADC errors (ESADC/ECADC) is deactivated. The detection of ADC errors (ESADC/ECADC) is activated.
16	MVLOW	1	Bit	0 1	The detection of vector errors (EVLOW) is deactivated. The detection of vector errors (EVLOW) is activated.
15:14	GAIN1:0	CFGGAIN (Pin) 00 (EEPROM)	Binary	00 01 10 11	Nominal amplitude 660mV$_{pp}$ Nominal amplitude 330mV$_{pp}$ Nominal amplitude 160mV$_{pp}$ Nominal amplitude 50mV$_{pp}$ → chapter 7.1
13:11	DH2:0	00 & CFGDH (Pin) 001 (EEPROM)	Unsigned	DH	Threshold digital hysteresis. The value ”0” deactivates the digital hysteresis → chapter 7.3.2
10:8	TPP2:0	0 & CFGTPP (Pin) 001 (EEPROM)	Unsigned	TPP	Minimum edge distance $t_{pp} = 2^{TPP} / f_{OSZ}$ → chapter 7.3.2, 7.4
7:5	MODE	0 & CFGMODE (Pin) 000 (EEPROM)	Binary	000 001 010 011 100	ABZ output: standard ABZ ABZ output: sensor adjust 1 ABZ output: sensor adjust 2 ABZ output: sensor adjust Z ABZ output: MC / DSP → chapter 7.6
4	Z4	0	Bit	0 1	The width of the zero signal Z is one increment = ¼ period. The width of the zero signal Z is four increments = 1 period. → chapter 7.3.3
3:2	IR3:2	10 (256-fold)	Binary	00 01 10	Base interpolation rate 200 → IRATE = 200 / 100 / 50 / 25 Base interpolation rate 160 → IRATE = 160 / 80 / 40 / 20 Base interpolation rate 256 → IRATE = 256 / 128 / 64 / 32
1:0	IR1:0	00	Binary	00 01 10 11	Interpolation rate = Base interpolation rate / 1 → IRATE = 200 / 160 / 256 Interpolation rate = Base interpolation rate / 2 → IRATE = 100 / 80 / 128 Interpolation rate = Base interpolation rate / 4 → IRATE = 50 / 40 / 64 Interpolation rate = Base interpolation rate / 8 → IRATE = 25 / 20 / 32

ⓘ For recommended configuration of the register *CFG1* *see chapter 7.5 The interpolation rates 50 and 25 (IR3:0 = 0010 resp. 0011) may only be used in counter mode. The ABZ signals are invalid then.*

CFG2	Configuration 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DISLP	LP1	LP0	PHBER	PH3	PH2	PH1	PH0	-	-	-	OFFSCTL	OFFSCTL	GAINCTL	GAINCTL	DISCTL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ASYNC	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0	VT1	VT0	T7	T6	T5	T4	T3	T2	T1	T0

Bit	Name	Reset value	Format	Value	Meaning
31	DISLP	0	Bit	0 1	The analog low pass filter is active The analog low pass filter is inactive
30:29	LP(1:0)	00	Binary	00 01 10 11	The analog low pass filter has a cut off frequency (-1dB) from 450 kHz The analog low pass filter has a cut off frequency (-1dB) from 200 kHz The analog low pass filter has a cut off frequency of (-1dB) from 75 kHz The analog low pass filter has a cut off frequency (-1dB) from 10 kHz
28	PHBER	0	Bit	0 1	The setting range of the phase correction potentiometer is± 5° The step size is 0.7° The setting range of the phase correction potentiometer is ± 10°. The step size is 1.4°
27:24	PH3:0	000000	Binary	PH -8 -1 0 7	Setting value of the phase correction potentiometer Phase correction value = 0.7°·PH resp. phase correction value = 1.4°·PH → Bit 28 PHBER smallest setting value: Phase correction value = 0.7°(1.4°)·-7 = -4.9°(9.8)° centre setting value: Phase correction value = 0° centre setting value: Phase correction value = 0° largest setting value: Phase correction value = 0.7°(1.4°)·-7 = +4.9°(9.8)°
23:21	-	000	Binary	-	-
20:19	OFFSCTL	00	Binary	00 01 10 11	Default value for the settling time of the offset controller. This configuration must be selected if the sensor signal has a lower input frequency or is overlaid by noise, or the phase between sinusoidal and cosinusoidal signals cannot be fully adjusted using the phase correction potentiometer. Reduction of the settling time of the offset controller by a factor of approx. 2 Reduction of the settling time of the offset controller by a factor of approx. 4 Reduction of the settling time of the offset controller by a factor of approx. 8
18:17	GAINCTL	00	Binary	00 01 10 11	Default value for the settling time of the gain controller. This configuration must be selected if the sensor signal has a lower input frequency or is overlaid by noise, or the phase between sinusoidal and cosinusoidal signals cannot be fully adjusted using the phase correction potentiometer. Reduction of the settling time of the gain controller by a factor of approx. 2 Reduction of the settling time of the gain controller by a factor of approx. 4 Reduction of the settling time of the gain controller by a factor of approx. 8
16	DISCTL	0	Bit	0 1	The internal controller for gain and offset is activated. The internal controller for gain and offset is deactivated.
15	ASYNC	0	Bit	0 1	The data to be read are accepted into a 32-bit holding register synchronously to the internal sequence using the SPI word RD0/ST. The time of acceptance can be shifted relative to the sampling time using the value of SYNC. Data to be read are accepted asynchronously into a 32-bit holding register using the SPI word RD0/ST. The value of SYNC is not evaluated. → chapter 8.1.4
14:10	SYNC4:0	00000	Unsigned		Displacement of an SPI read access relative to the sampling time. To read the registers MVAL, CNT and ADC_x, any value can be set. The default value '00000' provides a small delay between the calculated count value and the data output at the SPI interface. To read the registers PHI, DPHI, BQ and CADC_x, a value of '00100' must be used. → chapter 8.1.4
9:8	VT1:0	00	Binary	00 01 10 11	$f_{VT} = f_{OSZ} / 2^6$ $f_{VT} = f_{OSZ} / 2^{10}$ $f_{VT} = f_{OSZ} / 2^{14}$ $f_{VT} = f_{OSZ} / 2^{16}$ Time constant for the timer. $t_{Timer} = (T+1)/f_{VT}$; If VT = T = 0, the timer is deactive. → chapter 7.7
7:0	T7:0	0x00	Unsigned	T	Time constant for the timer. $t_{Timer} = (T+1)/f_{VT}$; If VT = T = 0, the timer is deactive → chapter 7.7

CFG3	*Configuration 3*

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRE_MT															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSI	SPISLOW	-	-	-	-	ZDEL	DISZ	ZMODE	ZMODE	PHIOUTZ	ZPOS4	ZPOS3	ZPOS2	ZPOS1	ZPOS0

Bit	Name	Reset value	Format	Value	Meaning
31:16	PRE_MT	0x0000	Unsigned	PRE_MT	Pre-load value of the multi-turn counter → chapter 7.9
15	SSI	0	Bit	0 1	For the IC GC-IP201B BISS is used as digital interface For the IC GC-IP201B SSI is used as digital interface There is only an evaluation of the bit if the interface BISS/SSI was activated via SEN=Low during Reset. In the IC GC-IP201 the interface BISS cannot be activated. → chapter 6.1
14	SPISLOW	1	Bit	0 1	SPI operates with maximum clock frequency of 25 MHZ. There is no filtering of the input signals. SPI operates with maximum clock frequency of $f_{OSZ}/4$. There is a filtering through 2-times sampling of the SPI input signals and the SPI clock.
13:10	-	0000	Binary	-	-
9	ZDEL	0	Bit	0 1	Default value Additional internal delay of the reference point signal of about $32/f_{OSZ}$
8	DISZ	0	Bit	0 1	Reference point processing is active Reference point processing is inactive
7:6	ZMODE	00	Binary	00 01 10 11	Reference point mode incremental Reference point mode trigger Reference point mode adjust Z Reference point mode distance coded → chapter 7.3.3, 7.6.3, 7.7
5	PHIOUTZ	0	Bit	0 1	The read register PHI is related to sinusoidal and cosinusoidal 0° equates the sine signal zero passage and the cosine signal maximum value The read register PHI is related to the set reference point position 0° equates ZPOS4:0
4:0	ZPOS4:0	00100 (45°)	Unsigned	ZPOS	Configuration of the analog reference point position related to the sine signal Position Reference point = approx. ZPOS · 11.25° → chapter 7.3.3

PRE_ST	Preload value counter

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRE(31:16)															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRE(15:0)															

Bit	Name	Reset value	Format	Value	Meaning
31:0	PRE	0x0000	Unsigned	PRE	Preload value of the counter → chapter 7.9

CFGBISS	Configuration SSI and Configuration BISS

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	SSI13	RING	SSITO(11:0)											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MTBIT		GRAY	STBIT					-	READ32	CLK10	BISSTO(4:0)				

Bit	Name	Reset value	Format	Value	Meaning
31	-	0	Bit	-	-
30	-	0	Bit	-	-
29	SSI13	1		0 1	25 Bit SSI data 13 Bit SSI data → chapters 7.8, 8.3 → Table 24
28	RING	1	Bit	0 1	SSI Ring mode inactive SSI Ring mode active → chapter 8.3
27:16	SSITO	797 decimal	Unsigned	SSITO	Configuration SSI timeout parameter to 1µs....20µs. $Timeout = (SSITO+3)/f_{OSZ}$ resp. $SSITO = (Timeout \cdot f_{OSZ}) - 3$ example: f_{OSZ} = 40MHz → SSITO = 37(1µs) … 797(20µs) → chapter 8.3
15:14	MTBIT	00	Binary	00 01 10 11	0 Bit multi-turn counter within the position data 8 Bit multi-turn counter within the position data 12 Bit multi-turn counter within the position data 16 Bit multi-turn counter within the position data → chapter 7.8 → Table 24
13	GRAY	1	Bit	0 1	Position data (multi-turn- and single-turn counter) are binary coded Position data (multi-turn- and single-turn counter) are gray-coded
12:8	STBIT	30 decimal	Binary	STBIT	Resolution of the single-turn value within the position data in Bit, Range: 8-30Bit Attention! The number of transmitted bits results from Table 24
7	-	0	Bit	-	-
6	READ32	0	Bit	0 1	Read access via BISS in 8 bit-format. Usable for read out of configuration registers Read access via BISS in 32 Bit-Format. It is required to read always the 4 following addresses starting with the least significant address (divisible by 4). Required for reading of the data registers.
5	CLK10	1	Bit	0 1	f_{OSZ} < 10MHz f_{OSZ} ≥ 10MHz
4:0	BISSTO	10 decimal	Unsigned	BISSTO	Configuration BiSS timeout parameter to 12µs....40µs. $Timeout = 2^{BISSTO}/f_{OSZ}$ bzw. $BISSTO = log2(Timeout \cdot f_{OSZ})$ Example: f_{OSZ} = 40MHz → BISSTO = 9(12.8µs) or 10(25.6µs) → chapter 8.2

ⓘ *For securing a correct BiSS functionality, this register has to be configured via SPI within the EEPROM. For EEPROM programming the bit `CLK10` has to be set to the range of the existing clock frequency.*

CNTRLG	Controller: Gain correction value

When writing the bits 25-16, the bits 23-16 must be written first. Subsequently, the whole correction value is refreshed in the register by writing of the bits 25-24.
When writing the bits 9-0, the bits 7-0 must be written first. Subsequently, the whole correction value is refreshed in the register by writing of the bits 9-8.

Please note that the correction values are changed automatically by the IC with active signal control.

31	30	29	28	27	25	25:16
0	0	0	0	0	0	CNTRLG_S

15	14	13	12	11	10	9:0
0	0	0	0	0	0	CNTRLG_C

Bit	Name	Reset value	Format	Value	Meaning
25:16	CNTRLG_S	0x100	Unsigned	CNTRLG	CADC_S = [2·ADC_S + CNTRLO_S] · (0.5 + CNTRLG_S/512) CADC_C = [2·ADC_C + CNTRLO_C] · (0.5 + CNTRLG_C/512) 1 increment = 2^{-9}
9:0	CNTRLG_C	0x100	Unsigned	0x000 0x100 0x1FF	Minimum value; the offset-corrected ADC values of the sinusoidal signal are multiplied by 0.5. Mean value; the offset-corrected ADC values of the sinusoidal signal are multiplied by 1.0. Maximum value; the offset-corrected ADC values of the sinusoidal signal are multiplied by 1.5

CNTRLO	Controller: Offset correction value

When writing the bits 31:16, the bits 23-16 must be written first. Subsequently, the whole correction value is refreshed in the register by writing of the bits 31-24. If the value to be written lies outside the valid range of -340...+339, the correction register is no longer refreshed, and the bit ESOFF in the register STAT/ERR is set.

When writing the bits 15-0, the bits 7-0 must be written first to address 0x18. Subsequently, the whole correction value is refreshed in the register by writing of the bits 15-8. If the value to be written lies outside the valid range of -340...+339, the correction register is no longer refreshed, and the bit ECOFF in the register STAT/ERR is set.
Please note that the correction values are changed automatically by the IC with active signal control.

31:16
CNTRLO_S

15:0
CNTRLO_C

Bit	Name	Reset value	Format	value	Meaning
31:16	CNTRLO_S	0x0000	Signed	CNTRLO	CADC_S = [2·ADC_S + CNTRLO_S] · (0.5 + CNTRLG_S/512) CADC_C = [2·ADC_C + CNTRLO_C] · (0.5 + CNTRLG_C/512) 1 increment = 2^{-11}·$U_{DiffNom}$·1.5 ($U_{DiffNom}$ → Table 11)
15:0	CNTRLO_C	0x0000	Signed		
				0xFEAC	Minimum value -340
				0x0000	Mean value 0; no offset correction
				0x0153	Maximum value +339

ADC	ADC value

31:16
ADC_S

15:0
ADC_C

Bit	Name	Reset value	Format	value	Meaning
31:16	ADC_S		Signed	0xFE00	Minimum value -512; corresponds to a differential voltage of approx. -495mV aat the input of the instrument amplifier (@GAIN=00)
				0x0000	Mean value 0; corresponds to a differential voltage of approx. 0mV at the input of the instrument amplifier
15:0	ADC_C		Signed	0x01FF	Maximum value +511; corresponds to a differential voltage of approx. +495mV at the input of the instrument amplifier (@GAIN=00) → chapter 7.1 → Table 11

CADC	Corrected ADC value

31	30	29:16
VZ(CADC_S)	0	Abs(CADC_S)

15	14	13:0
VZ(CADC_C)	0	Abs(CADC_C)

Bit	Name	Reset Value	Format	Value	Meaning
31	VZ(CADC_S)		Bit	0	Corrected ADC value, sinusoidal ≥ 0
				1	Corrected ADC value, sinusoidal < 0
29:16	Abs(CADC_S)		Unsigned		Corrected ADC value sinusoidal (absolute value)
				0	Minimum value
				0x7FF	Maximum value
15	VZ(CADC_C)		Bit	0	Corrected ADC value, cosinusoidal ≥ 0
				1	Corrected ADC value, cosinusoidal < 0
13:0	Abs(CADC_C)		Unsigned		Corrected ADC value cosinusoidal (absolute value)
				0	Minimum value
				0x7FF	Maximum value

Bit	Name	Reset Value	Format	Value	Meaning
31:16	CADC_S		Sign + Absolute value		Corrected ADC value, sinusoidal CADC_S = [2·ADC_S + CNTRLO_S] · (0.5 + CNTRLG_S/512)
15:0	CADC_C		Sign + Absolute		Corrected ADC value, cosinusoidal CADC_C = [2·ADC_C + CNTRLO_C] · (0.5 + CNTRLG_C/512)

Bit	Name	Reset Value	Format	Value	Meaning
			value		

IP1 Interpolation register 1 – angle value / speed

31:16
DPHI

15:0
PHI

Bit	Name	Reset Value	Format	Value	Meaning
31:16	DPHI		Signed	DPHI	The value DPHI is the difference in the phase angle of sinusoidal and cosinusoidal signals between two samplings. The range of values is dependent on the set interpolation rate. Using that value it is possible to get information about the speed of the measuring system. -95 ≤ DPHI < 95 for the interpolation rates **256** ,128, 64, und 32 -74 ≤ DPHI < 74 for the interpolation rates **200**,100, 50 und 25 -60 ≤ DPHI < 60 for the interpolation rates **160**, 80, 40 und 20 DPHI = 32 · Base interpolation rate · f_{Input}/f_{OSZ}
15:0	PHI		Unsigned	0x0000 Maximal	The phase angle of sinusoidal and cosinusoidal signals is 0°. The phase angle of sinusoidal and cosinusoidal signals is 360° - ε. The maximum value is dependent on the set interpolation rate. Maximum value 255 for the interpolation rates 256,128,64 and 32 Maximum value 199 for the interpolation rates 200,100, 50 and 25 Maximum value 159 for the interpolation rates 160, 80, 40 and 20 Using CFG3/PHIOUTZ the related value (0°) can be shift.

IP2 *Interpolation register 2 – angular value / controller value*

31:16
BQ

15:0
PHI

Bit	Name	Reset Value	Format	Value	Meaning
31:16	BQ		Unsigned	BQ	The value BQ contains the deviation of the gain and offset controller from the setpoint. If offset and gain are adjusted completely, the value of this register is 160.
15:0	PHI		Unsigned	0x0000 Maximal	The phase angle of sinusoidal and cosinusoidal signals is 0°. The phase angle of sinusoidal and cosinusoidal signals is 360° - ε. The maximum value is dependent on the set interpolation rate. Maximum value 255 for the interpolation rates 256,128,64 and 32 Maximum value 199 for the interpolation rates 200,100, 50 and 25 Maximum value 159 for the interpolation rates 160, 80, 40 and 20

CMD Command

7	6	5	4	3	2	1	0
-	-	SETHWA	WCFG	RESIC	CLRZ	RESCTL	RESCNT

Bit	Name	Reset Value	Format	Value	Meaning
5	SETHWA			1	The pins HWA3, HWA2, HWA1 and HWA0 are read into the IC as hardware addresses. If several ICs are to be connected to one SPI interface, this command **must** be sent first to all connected ICs. Runs in BISS mode during the initialisation automatically to set HWA as LSB of the serial number → chapter 8.1.2
4	WCFG			1	The contents of the registers CFG1, CFG2, CFG3, CNTRLG and CNTRLO are transferred to the EEPROM The register content of CFGBISS will not be transferred to the EEPROM.
3	RESIC			1	The IC will be reset and configured new → chapter 6.1
2	CLRZ			1	The status bit ZSTAT is reset. For the reference point modes „adjust ZPOS“ and „distance coded“ a new evaluation will be started. → chapter 11.3
1	RESCTL			1	The internal controller for gain and offset is reset, i.e. all correction values for offset and gain are set to the centre of their range of values.
0	RESCNT			1	The count value is set to the register content of PRE_ST. The multi-turn counter will be set with PRE_MT from the register CFG3. All error flags in the status register are reset, and the status bit ZSTAT is also reset. or the reference point modes „adjust ZPOS“ and „distance coded“ a new evaluation will be started. → chapters 7.9, 11.3

EEP	EEPROM interface

read

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-					-	-	AUT	EER	EEPVALID	EWR	EEPBSY	RSV

15:0
EEPDAT

Bit	Name	Reset Value	Format	Value	Meaning
21	AUT	0	Bit		The bit is reserved for test purposes.
20	EWR	0	Bit	0 1	No EEPROM erase command active EEPROM erase command active
19	EEPVALID	0/1	Bit	0 1	Validation identifier 0x134A at address 0x00 not found Validation identifier 0x134A at Address 0x00 found. EEPROM content were load to the related register after reset. → chapter 6.1
18	EWR	0	Bit	0 1	No EEPROM write access active EEPROM write access active
17	EEPBSY	0	Bit	0 1	No EEPROM access active EEPROM access active; No further command must be sent to the EEPROM.
16	RSV	0	Bit		The bit is reserved for further application
15:0	EEPDAT	0x0000	Binary		Read EEPROM data

write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	EEPOPC			EEPADR							

15:0
EEPDAT

Bit	Name	Reset Value	Format	Value	Meaning
26:24	EEPOPC	0000	Binary	000 001 010 100 other	EEP OPCode. Writing to this register triggers an EEPROM access. The register must not be written if the bit EEPBSY is set. EEPADR and EEPDAT must be valid. NOP – no action WRITE – 16 Bit write READ – 16 Bit read ERASE – 16 Bit erase Undefined behaviour. The EEPROM content can be lost. → chapter 8.4, 11.4
23:16	EEPADR	0x00	Binary		EEPROM address. To program or read the EEPROM, the address must be written to this register before activating the OPCode. The register must not be written if the EEPBSY bit in the register EEPSTAT is active.
15-0	EEPDAT	0x0000	Binary		EEPROM data. To program the EEPROM, the data must be written to this register before activating the OP code. Once the EEPROM has been read, this register will receive the EEPROM data. The register must not be written if the EEPBSY bit is active.

MANUFACTURE	Manufacturer settings

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV3								RSV2							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV1								RSV0							

Bit	Name	Reset Value	Format	Value	Meaning
31:24	RSV3	0	Binary		Must not be changed.
23:16	RSV2	0	Binary		Must not be changed.
15:8	RSV1	0	Binary		Must not be changed, in order not to affect the functionality of the EEPROM
7:0	RSV0	62dez	Binary		Must not be changed, in order not to affect the functionality of the EEPROM

BiSS device code	Device code

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MTBIT								STBIT							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV_CLASS								ASICID				ASICREV			

Bit	Name	Reset value	Format	Value	Meaning
31:24	MTBIT	0x00	Hexadecimal	0x00 0x08 0x0C 0x10	Number of the multi-turn counter bits in the single-cycle-data MT: 0; ST = 8...30 MT: 8; ST = 8...24 MT: 12; ST = 8...20 MT: 16; ST = 8...16
23:16	STBIT	0x1E	Hexadecimal	0x08 – 0x1E	Number of single-turn counter bits in the single-cycle-data
15:8	DEV_CLASS	0x01	Hexadecimal		Device class
7:4	ASICID	0101	Binary	0101	IC identifier GC-IP201/GC-IP201B
3:0	ASICREV		Binary		Silicon revision of the IC

BiSS timeout	BiSS timeout register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	TO		

Bit	Name	Reset value	Format	Value	Meaning
2:0	TO	000	Binary	000	Timeout

BiSS manufacturer ID	Manufacturer identification

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAN_ID_1								MAN_ID_0							

Bit	Name	Reset value	Format	Value	Meaning
15:8	MAN_ID_1	0x43	Hexadecimal	0x43	Manufacturer ID „C“
7:0	MAN_ID_0	0x47	Hexadecimal	0x47	Manufacturer ID „G"

10 Electrical specifications

Table 35: Absolute maximum ratings

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
VDDA	Analog supply voltage			3.60	V
VDD	Digital supply voltage			3.60	V
T	Operating temperature	-40		150	°C
TS	Storage temperature	-55		150	°C
V(AIN)	Voltage at the analog inputs	-0.3		VDDA+0.3	V
V(DIN)	Voltage at the digital inputs	-0.3		VDD+0.3	V
ESD	ESD sensitivity (HBM)			2	kV

Table 36: Operating conditions

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
VDDA	Analog supply voltage	3.15	3.30	3.45	V
VDD	Digital supply voltage	3.15	3.30	3.45	V
I(VDDA)	Current consumption analog		11		mA
I(VDD)	Current consumption digital		$0.42 \cdot f_{OSZ} + 1.3$		mA
T	Operating temperature	-40		150 [1)]	°C

Table 37: Characteristic values of the oscillator / Reset

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
f_{OSZ} (internal)	Internal clock frequency: Frequency	35	40 [1)]	45 [1)]	MHz
f_{OSZ} (external)	External clock frequency: Frequency	4		40 [1)]	MHz
TH/TL	External clock : duty cycle	40	50	60	%
t_{INIT}	Initialisation time Time between `NRES` rising and Ready (`MISO`,`NERR`)	30	40	50	ms

[1)] For T > 85°C and BiSS operation the maximum clock frequency is f_{OSZ} = 27MHz.

Table 38: Characteristic values interpolation

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
f_{IP}	Input frequency, internal controller disabled (@DISCTL = 1)	0		440	kHz
f_{IP}	Input frequency, internal controller enabled	0		410	kHz
IRATE	Interpolation rate	20		256	Increments
CTRL(A)	Control range amplitude control	60		120	%VINNOM[2)]
CTRL(O)	Control range offset control	-15		15	%VINNOM[2)]
VTH(INP)	Threshold voltage vector monitoring		30		%VINNOM[2)]
EABS	Absolute angle error [1)]		±0.6	1.0	Increments
EDIFF	Differential angle error [1)]		±0.3		Increments
tpp	Minimum edge distance A/B	$1/f_{OSZ}$		$128/f_{OSZ}$	ns
tp(TRG)	Pulse width trigger signal	$3/f_{OSZ}$			ns
tp(Teach)	Pulse width Zero/Teach-Signal	$32768/f_{OSZ}$			ns
td(CNT)	Delay time analog input to `CNT` resp.. `POSIT` (@DISLP=1)		$90/f_{OSZ}$ + 100		ns
td(ABZ)	Delay time analog input to A/B (@DISLP=1)		$122/f_{OSZ}$ + 100		ns

[1)] In case of adjusted phase angle between sine and cosine
[2)] Nominal value of the differential voltage of SINP-SINN resp. COSP-COSN

Table 39: Characteristic values digital

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
VOH	Output voltage H	80			%VDDIO
VOL	Output voltage L			0.4	V
VIH	Input voltage H	70			%VDDIO
VIL	Input voltage L			30	%VDDIO
I(DIG1)	Output current digital			6	mA
I(DIG2)	Output current digital at MISO and NERR			12	mA
R(PU)	Internal pull-up resistors	90k		210	KΩ
R(PD)	Internal pull-down resistors	75k		250	KΩ

Table 40: Characteristic values analog

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
Z(AIN)	Input impedance		1GΩ||8pF		
Gain	Gain (as per Table 9) @1kHz	97	100	103	%
fg	Limit frequency (as per. Table 10) @CFG2/DISLP = 0	90	100	110	%
fg_{bypass}	Limit frequency @CFG2/DISLP = 1	460			kHz
fg_{MATCH}	Deviation of the limit frequencies between the channels	-1	0	+1	%
V(AIN)	Voltage at the analog inputs	0.35		VDDA-1.0	V
CMIR	Common-mode input voltage → Figure 5		1.1		V
CMRR	Common-mode rejection ratio (@ f < 1kHz, CFG1/GAIN = 11)	65			dB
V(V0)	Voltage at Pin V0 / DC-voltage at SMON/CMON	1.08	1.1	1.12	V
VMON	AC-voltage at SMON/CMON @ Nominal amplitude		1.27		V_{pp}
I(V0)	Output current on pin V0			1	mA
CL(V0)	Capacitive load on pin V0			300	pF
VTH(REF)	Switching point of the reference-point comparator[2)]	-1		1	mV
VH(REF)	Hysteresis reference-point comparator[2)]		15		%VINNOM[1)]
I(OUTX)	Output current on pin SMON/CMON			0.05	mA
CL(OUTX)	Capacitive load on pin SMON/CMON			50	pF
φK1	Phase correction in range (@ CFG2/PHBER = 0)	± 4.5	± 5	± 5.5	°
φK2	Phase correction in range (@ CFG2/PHBER = 1)	± 9	± 10	± 11	°

[1)] Nominal value of the differential voltage of SINP-SINN resp. COSP-COSN
[1)] Differential voltage of REFP-REFN

Table 41: Characteristic values EEPROM

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
$t_{READEEP}$	Read time @CFGBISS/CLK10 valid (any)	20		85 (250)	us
$t_{PROGEEP}$	Programming time / erase time	4		9	ms
$t_{RETENTIONEEP}$	Data storage @ T < 85°	10			years
$N_{ProgEEP}$	Programming cycles @ T = 25° @ T = 125°	10^4 10^3			

Table 42: Characteristic values SSI

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
f_{MA}	Clock frequency @ f_{OSZ} ≥ 4MHz @ f_{OSZ} ≥ 8MHz @ f_{OSZ} ≥ 10MHz @ f_{OSZ} ≥ 20MHz			2 3 4 5	MHz
t_D(MISO)	Delay time MA rising to SLO			25	ns
$t_{TIMEOUT}$	Time out → CFGBISS	$3/f_{OSZ}$	10	4095 / f_{OSZ}	us

Table 43: Characteristic values BISS

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
f_{MA}	Clock frequency			10	MHz
t_D(MISOBISS)	Delay time MA rising to SLO			20	ns
$t_{TIMEOUT}$	Time out → CFGBISS	$2/f_{OSZ}$	25	$2^{31}/f_{OSZ}$	us

Table 44: Characteristic values SPI @CFG2/SPISLOW=0

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
t_{HIGH}(SCK)	SPI clock, H-time	20			ns
t_{LOW}(SCK)	SPI clock, L-time	20			ns
t_S(SEN)	Setup time SEN falling before SCK rising	15			ns
t_H(SEN)	Hold time SEN rising after SCK falling	15			ns
t_S(MOSI)	Setup time MOSI before SCK rising	5			ns
t_H(MOSI)	Hold time MOSI after SCK rising	5			ns
t_D(MISO)	Delay time SCK **falling to** MISO @CL = 12 pF			20	ns
t_{ENA}(MISO)[1)]	Delay time SEN falling to MISO active			25	ns
t_D(nWAIT)	Delay time SEN rising to nWAIT active		60	70	ns
t(nWAIT-L)	Wait time after SEN rising	$2/f_{OSZ}$		$4/f_{OSZ}$ + 25	ns
	Wait time after SEN rising (synchronously reading)	$2/f_{OSZ}$		$36/f_{OSZ}$ + 25	ns
t(SEN-Wait)	Time between wait and the following access	0			ns

[1)] for non-reading commands the output MISO can be within the state Tristate (inactive)

Table 45: Characteristic values SPI @CFG2/SPISLOW=1

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
t_{HIGH}(SCK)	SPI clock, H-time	$2/f_{OSZ}$ + 25			ns
t_{LOW}(SCK)	SPI clock, L-time	$2/f_{OSZ}$ + 25			ns
t_S(SEN)	Setup time SEN falling before SCK rising	$1/f_{OSZ}$ + 25			ns
t_H(SEN)	Hold time SEN rising after SCK falling	$2/f_{OSZ}$ + 25			ns
t_S(MOSI)	Setup time MOSI before SCK rising	$1/f_{OSZ}$ + 25			ns
t_H(MOSI)	Hold time MOSI after SCK rising	5			ns
t_D(MISO@SPISLOW)	Delay time SCK **rising** to MISO	$3/f_{OSZ}$ + 25		$4/f_{OSZ}$ + 25	ns
t_{ENA}(MISO) [1)]	Delay time SCK falling to MISO active	$3/f_{OSZ}$		$4/f_{OSZ}$ + 25	ns
t_D(nWAIT)	Delay time SEN rising to nWAIT active	$3/f_{OSZ}$		$4/f_{OSZ}$ + 25	ns
t(nWAIT-L)	Wait time after SEN rising	$2/f_{OSZ}$		$4/f_{OSZ}$ + 25	ns
	Wait time after SEN rising (synchronously reading)	$2/f_{OSZ}$		$36/f_{OSZ}$ + 25	ns
t(SEN-Wait)	Time between wait and the following access	0			ns

[1)]for non-reading commands the output MISO can be within the state Tristate (inactive)

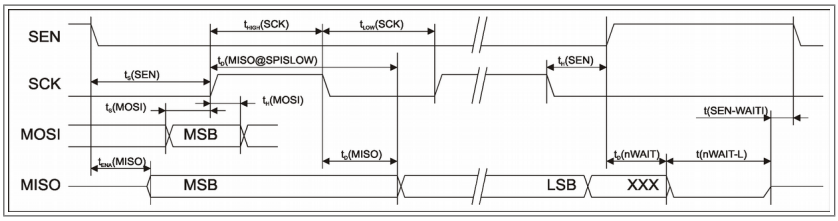


Figure 23: Timing SPI

11 Application note

11.1 Application circuit

As the interpolation ICs *GP-IP201(B)* contain two fast A/D converters, the same design rules applicable to A/D converter apply. All block capacitors are to be connected closely to the pad. The quality of the sensor power supply also influences the measuring accuracy of standard sensors. If necessary, additional LC filters must be included to the sensor power supply and to VDDA.
Supply voltages and ADC reference voltages must be connected according the following Table 46 and unused inputs / outputs according Table 47.

Table 46: IC connection voltages

Pin	Connection
VSSA	Analog ground
VSS, VSSIO, Exposed Pad	Digital ground
VDDA	Power supply voltage analog 3.3V Block capacitor 100nF against VSSA
VDD, VDDIO	Power supply voltage digital 3.3V Block capacitor 100nF against VSS/VSSIO
RL,RM,RH	Block capacitor 4.7uF against VSSA for each pin Block capacitor 10nF against VSSA for each pin
V0	Block capacitor 100nF against VSSA

Table 47: IC connection if unused input / output

Pin	Connection if unused
NRES	Pull- up 10k against VDDIO
CLK/CKSEL	VSS
SINN, COSN, REFN	V0
REFP	AVDD
CFGPIN	→ Table 6 and Table 9
CFGTPP, CFGGAIN, CFGDH	VSSIO
CFGMODE (Zero/Teach)	VSSIO if CFGPIN = H resp. VDDIO if CFGPIN = L
MISO/SLO	Pull-up 10k against VDDIO
MOSI/SLI	VSSIO
SCK/MA	VSSIO
SEN	VDDIO
NERR	Pull-up 10k against VDDIO
TM	VSS

Further:

- All block capacitors (refer to table below) have to be connected closely to the pad.
- Separate ground areas for VSSA and for VSS and VSSIO are required.
- The ground areas for VSSA and VSS/VSSIO must be connected at one point of the PCB.
- 10 kΩ Pull-up resistors are required at the pins NRES, NERR.
- 1 kΩ Pull-up resistors are required at the pin MISO/SLO.
- For using the SPI with high data rates, series resistors of 22...33Ω each at MOSI, MISO, SCK and SEN are useful.
- The digital outputs A, B and Z are designed with a maximum load of 12 mA . An external driver-IC is necessary to realize a differential RS422-interface. Those outputs can be configured to tri-state behaviour in case of an error. In dependence of the application pull-up resistors are required.
- For additional termination resistors between the pins SINP and SINN resp. between COSP and COSN the rules of the related sensor manufacturer are valid.
- Single-ended sensors are connected to the inputs SINP and COSP usually. Therefore, the DC reference level has to fit.
- The signal V0 can be used as DC reference level. That pin is designed with a maximum load of 1 mA. Short and low-capacitance lines are required. If necessary a special buffer OPA can be used.
- For save operation, all IC inputs have to be connected to defined levels. The internal pull-up resistors avoid undefined behaviour in case of open inputs only.

The design of the analog input circuit depends on the type of the sensor that is connected. The following sensors shows examples for the connection of different sensor types.

Sensor with differential output signals

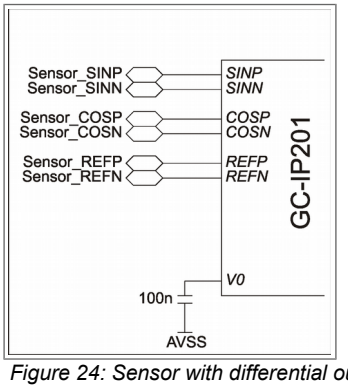


Figure 24: Sensor with differential output signals

- Error signal
- The amplitude of the sensor and the gain-factor of GC-IP201(B) are adapted by configuration bits GAIN(1:0).
- Reference level V0 is generated internally.

Sensor with a nominal amplitude of $1V_{pp}$ or $2V_{pp}$

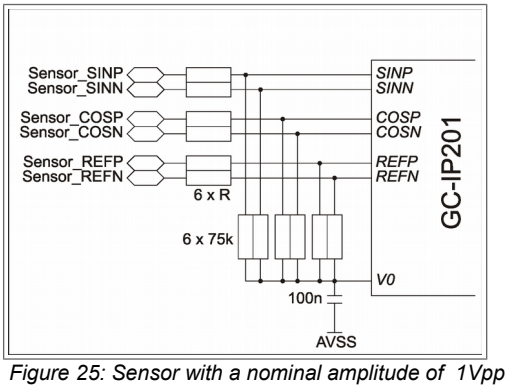


Figure 25: Sensor with a nominal amplitude of 1Vpp or 2Vpp

- The amplitude of the sensor and the gain-factor of GC-IP201(B) are adapted by configuration bits GAIN(1:0) to 660mVpp .
- Reference level V0 is generated internally..
- Resistors between the input signals are used as voltage dividers. Resistor value R: $R = (V_{Sensor} / 660mV - 1) \cdot 75\ k\Omega$
- The sensor amplitude and the centre voltage of the sensorwill divide in the ration R/75kΩ
- **Option: In case of 5V sensors the level shifter IC *GC-LS* can be used**

Sensor with single-ended output signals (1)

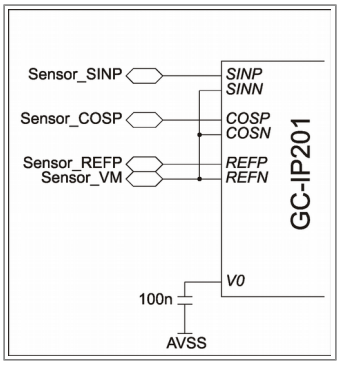


Figure 26: Sensor with single-ended output signals (1)

- The amplitude of the sensor and the gain-factor of GC-IP201(B) are adapted by configuration bits GAIN(1:0)
- Reference level V0 is generated internally.

Sensor with single-ended output signals (2)

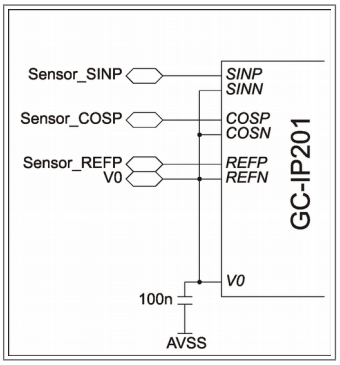


Figure 27: Sensor with single-ended output signals (2)

- The amplitude of the sensor and the gain-factor of GC-IP201(B) are adapted by configuration bits GAIN(1:0)
- Reference level V0 is generated internally and connected to the sensor.

Sensor containing antiparallel photodiodes
Adjustment of amplitude equality possible

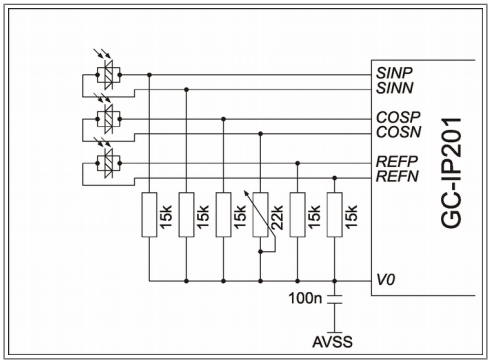


Figure 28: Sensor containing antiparallel photodiodes

- The amplitude of the sensor and the gain-factor of GC-IP201(B) are adapted by configuration bits GAIN(1:0) to 330mVpp.
- Reference level V0 is generated internally.
- The amplitude equality is adjusted by changing the amplitude of the cosine signal. The pins SMON and CMON are used for the measurement.
- The resistors between the input signals and V0 were used as I/U converter. The resistor value R will be calculated as: R_{FIX} = 330 mV / (2·I_{SENSOR}) and $P_{AMPL} \approx 1.5 \cdot R_{FIX}$
  → example: I_{SENSOR} = 11 μA_{pp}

Sensor containing photodiodes with common catode or common anode
Adjustment of amplitude equality and offset possible

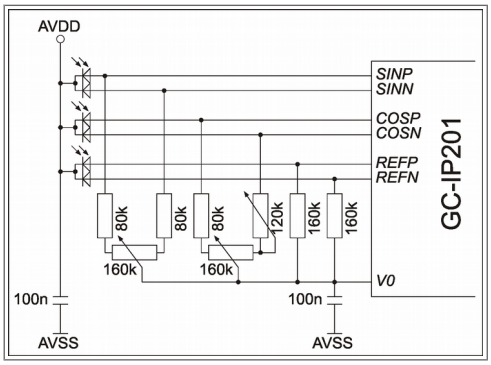


Figure 29: Sensor containing photodiodes with common catode or anode

- The amplitude of the sensor and the gain-factor of GC-IP201(B) are adapted by configuration bits GAIN(1:0) to 160mVpp.
- Reference level V0 is generated internally
- The amplitude equality is adjusted by changing the amplitude of the cosine signal. Thereafter the offset for both signals can be adjusted. The pins SMON and CMON are used for the measurement.
- The resistors between the input signals and V0 were used as I/U converter. The resistor value R will be calculated as: R = 160mV / (2·ISENSOR). That resistor is also used as potentiometer for o offset adjust :
  $P_{OFFS} \approx R$; $R_{FIX} \approx ½ R$; $P_{AMPL} \approx 1.5 \cdot R_{FIX}$
  →example: I_{SENSOR} = 0.5 µApp

Sensor with current outputs 11 μA_{pp}

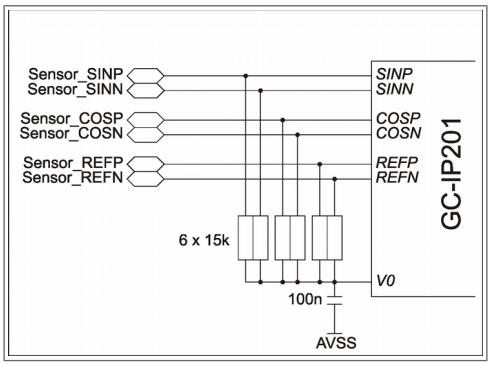


Figure 30: Sensor with current outputs 11 µApp

- The amplitude of the sensor and the gain-factor of GC-IP201(B) are adapted by configuration bits GAIN(1:0) to 330mVpp.
- Reference level V0 is generated **internally**.
- The resistors between the input signals and V0 were used as I/U converter. The resistor value R will be calculated as R = 330mV / (2·ISENSOR)
  → Example: I_{SENSOR} = 11 μA_{pp}

The following figures show examples for the connection of different interfaces at the output.

ABZ output / configuration via pin

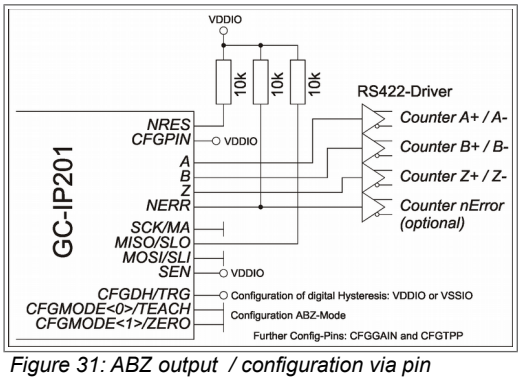


Figure 31: ABZ output / configuration via pin

- Nominal amplitude, minimum edge distance, hysteresis and ABZ mode will be set via configuration pins, all other configuration will be set according Table 9 .

ABZ output / configuration via EEPROM

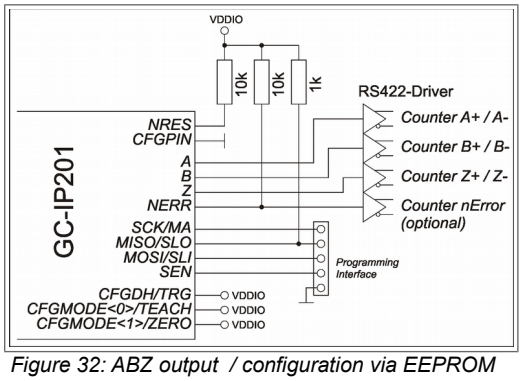


Figure 32: ABZ output / configuration via EEPROM

- IC configuration from the internal EEPROM
- SPI interface is used as programming interface for the EEPROM
- The lines for `MOSI`, `SEN` and `SCK` have to be kept very short. Otherwise external pull-up resistors (10 kΩ) are recommended.

SPI interface via LVDS

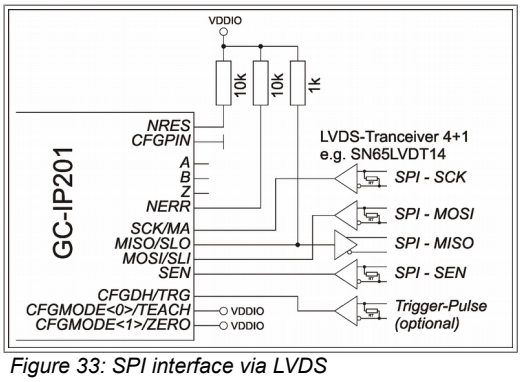


Figure 33: SPI interface via LVDS

- IC configuration from the internal EEPROM or via SPI
- LVDS driver for longer lines and higher clock rates
- A optional signal will be used for trigger

SPI interface via USB an PC

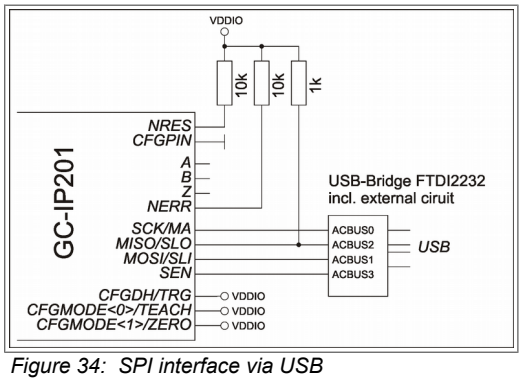


Figure 34: SPI interface via USB

- IC configuration from the internal EEPROM or via SPI
- SPI interface will be controlled via bridge-IC from PC-Software directly.

BiSS interface

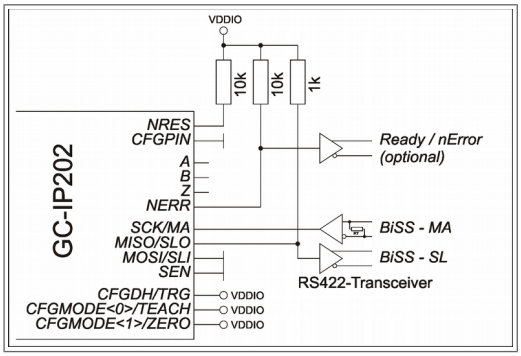


Figure 35: BiSS interface

- IC configuration from the internal EEPROM
- BiSS interface operates with a point to point connection
- An optional additional signal signalised the end of initialisation of the GC-IP201B resp. error.

SSI interface

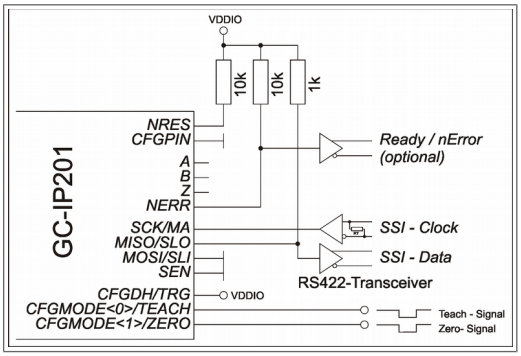


Figure 36: SSI interface

- IC configuration from the internal EEPROM
- An optional additional signal signalised the end of initialisation of the GC-IP201B resp. error.
- The teach and the zero function will be triggered by LVCMOS-pulses

SPI interface to a micro controller

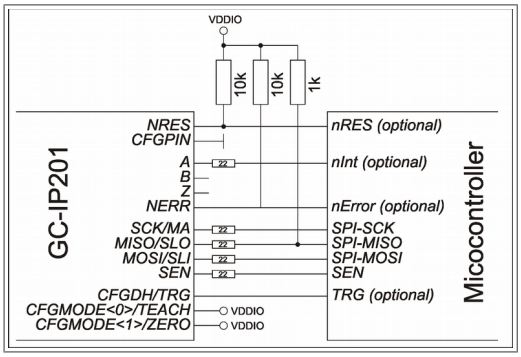


Figure 37: SPI interface t a micro controller

- IC configuration from the internal EEPROM or via SPI
- The SPI interface will be controlled by the micro controller firmware
- An optional additional signal is used as trigger, a further Signal is used as interrupt to the micro controller
- The interpolation IC will be reset from the micro controller optional

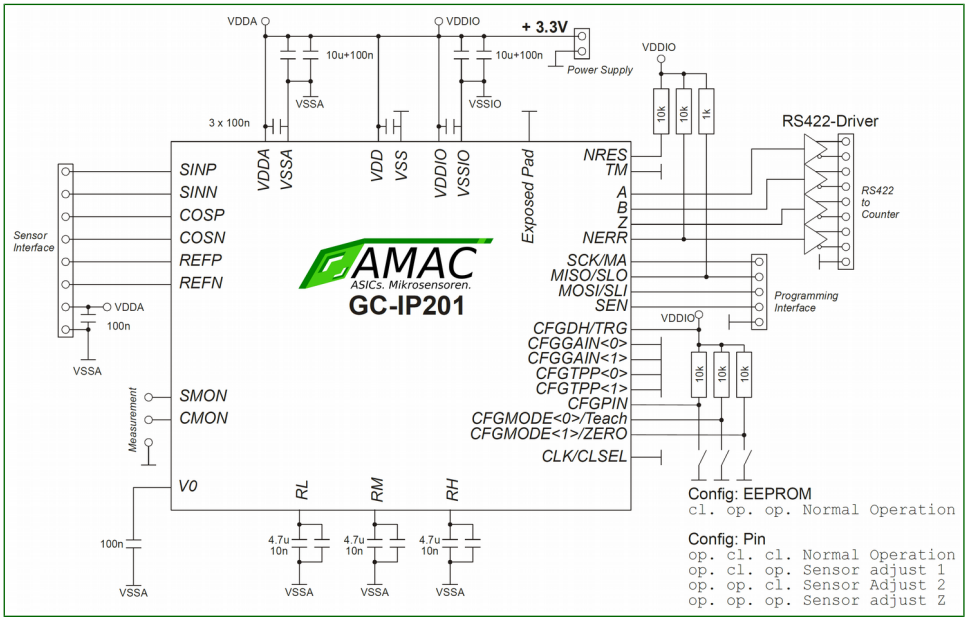


Figure 38: Minimal application

- IC configuration from the internal EEPROM
- For sensor adjust the configuration will be activated via pin. Afterwords, the ABZ signal mode can be set through the bit `CFGMODE` according to chapter 7.6.4.
- SPI interface is used as programming interface for the EEPROM.
- The lines for `MOSI`, `SEN` and `SCK` have to be kept very short. Otherwise external pull-up resistors (10 kΩ) are recommended.

For further information please ask for circuit diagram and layout of the demo board „GP-IP201“ per E-Mail at support@amac-chemnitz.de.

11.2 Fast equidistant measuring via SPI

The GC-IP201(B) supports fast equidistant measuring via SPI interface. There are different configuration options which can be chosen according to the following processing unit.

Table 48: Equidistant measuring

Time base	Timer	Pin `TRG`	Interface SPI	Remark
From the GC-IP201(B)	Time base	For asynchronous trigger events	ASYNC mode	Reading of the measured values via SPI must be completed within the timer interval. The signal `nINT` on output `A` can be used for synchronisation of further components.
From the SPI interface	Inactive	For asynchronous trigger events	SYNC mode	There is no jitter if `SEN` is activated with $N \cdot 32/f_{OSZ}$. An exact synchronisation of more IC is possible.
External	Inactive	Time base	ASYNC mode	Jitter: $32/f_{OSZ}$. Reading of the measured values via SPI must be completed within the timer interval.An exact synchronisation of more IC is possible.

The diagram below shows an example for a timer-controlled equidistant measurement using the signal `nINT`.

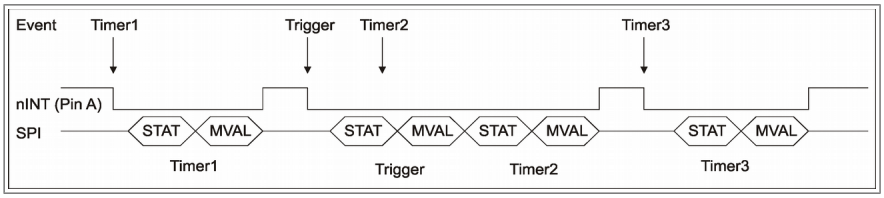


Figure 39: Example for a timer / trigger

11.3 Program flow

The use of trigger and sensor monitoring of the GC-IP201(B) happens in relation to the internal registers `MVAL` and `STAT`. Following program loop can be implemented:

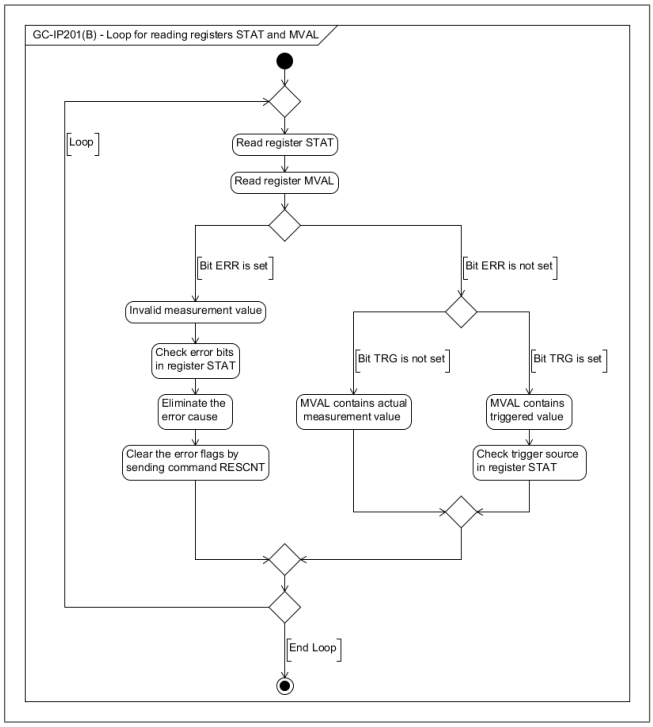


Figure 40: Program loop for read out of MVAL and STAT

The program loop can be extended for reference point position adjustment and for processing of distance coded reference marks:

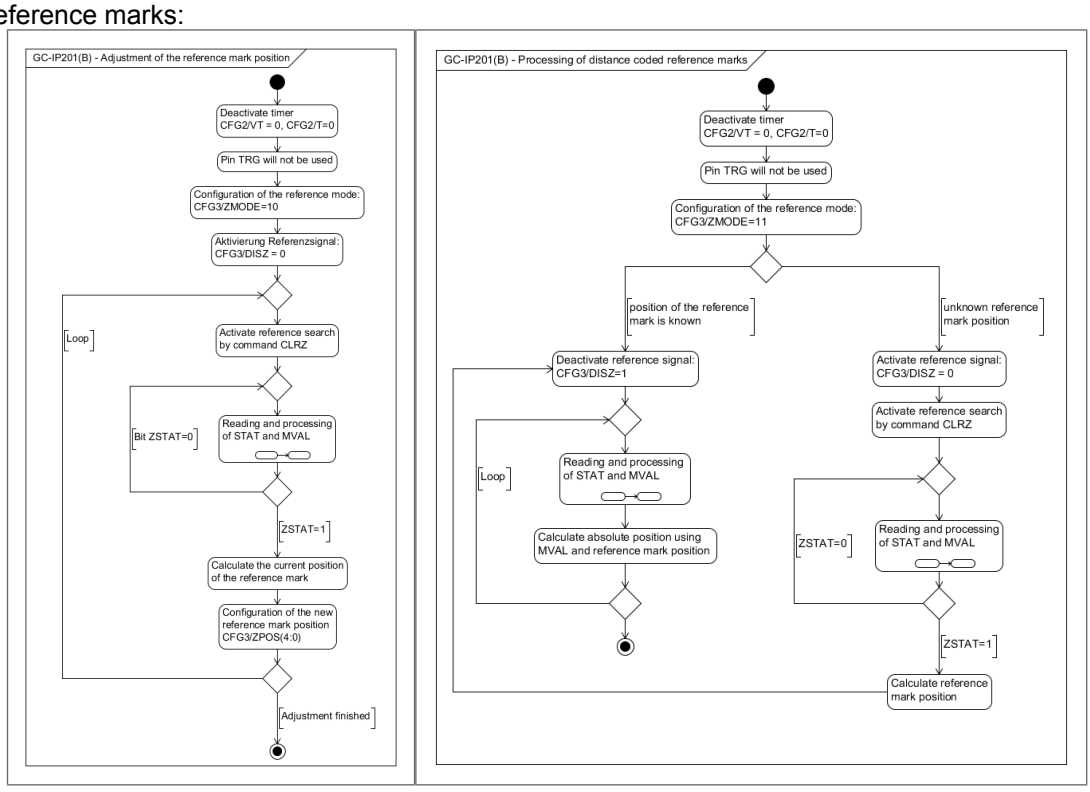


Figure 41: extended program loop for ZMODE 10 and 11

Refer to chapters 7.6.3 and 11.5.

11.4 EEPROM

The access to the internal EEPROM occurs via an internal interface, which controls the access to the register `EEP`:

- The bit `EEPBSY` must be erased before reading access
- Write access to `EEPOPC` (Byte 3) starts the EEPROM operation. The content of `EEPADR` and `EEPDAT` must be valid.
- Invalid OP codes must not be used!

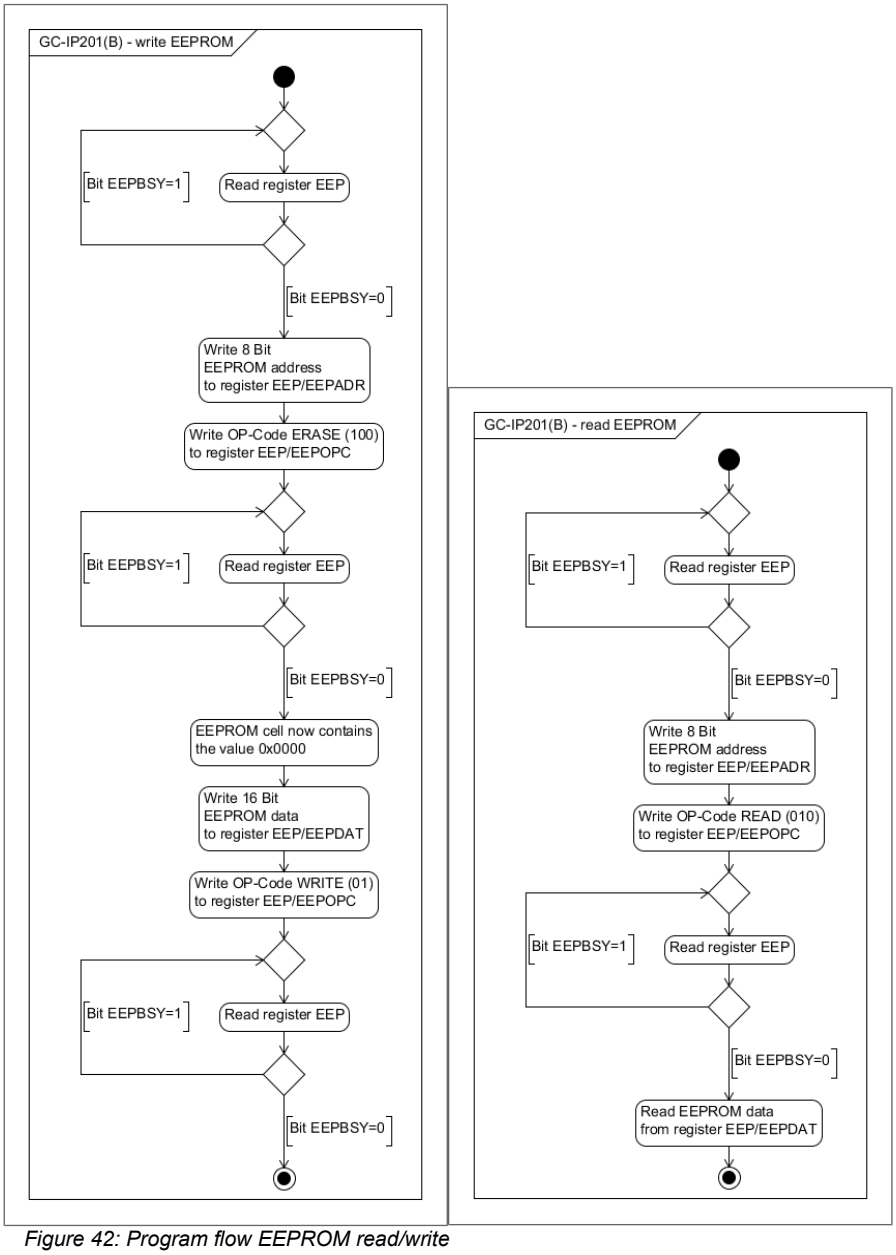


Figure 42: Program flow EEPROM read/write

11.5 Distance coded reference marks processing

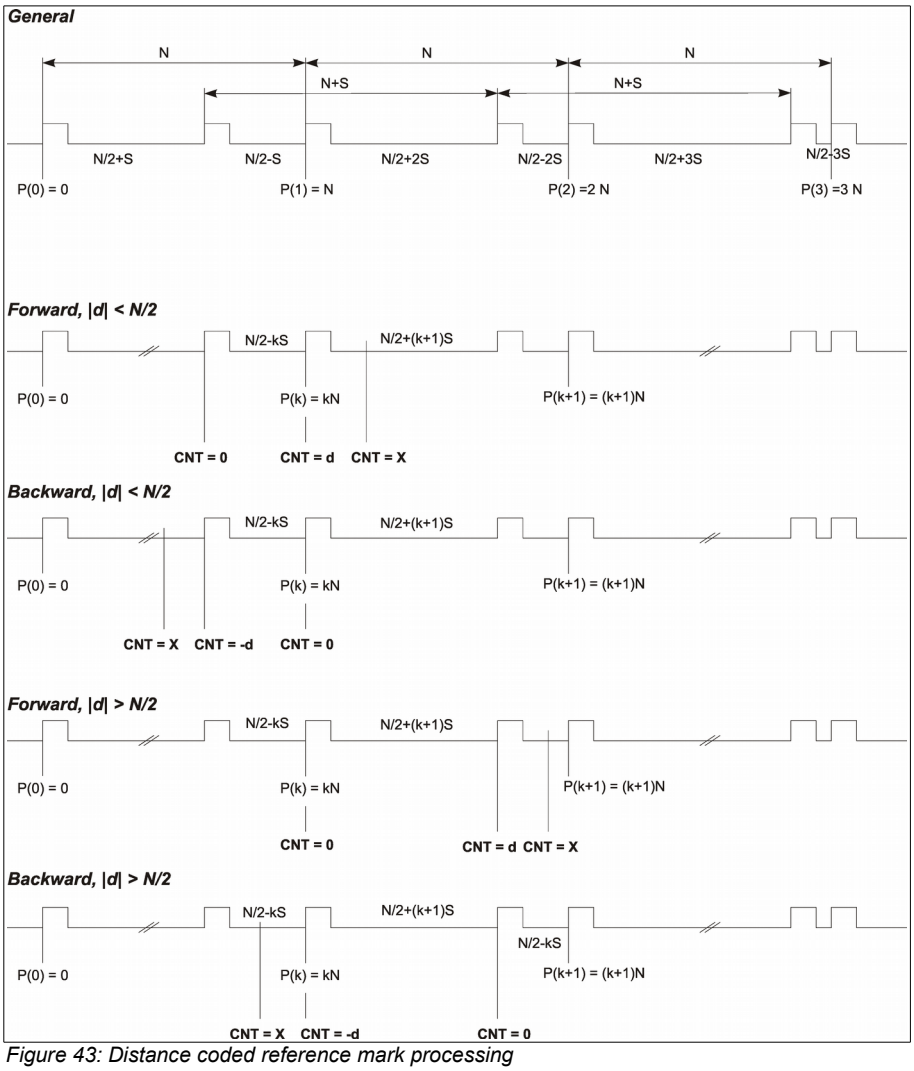


Figure 43: Distance coded reference mark processing

Table 49: Distance coded reference mark processing

0<d< ½·N Figure 43-1	-½·N<d<0 Figure 43-2	½·N<d Figure 43-3	d<-½·N Figure 43-4
D = d/IRATE·M	D = d/IRATE·M	D = d/IRATE·M	D = d/IRATE·M
D = (N/2-k·S)	D = -(N/2-k·S)	D = N/2+(k+1)·S	D = -N/2-(k+1)·S
P = N/S·(N/2-D)	P = N/S·(N/2+D)	P = N/S·(D-N/2)-N	P = -N/S·(D+N/2)-N
PX = P-D+X/IRATE·M	PX = P+X/IRATE·M	PX = P+X/IRATE·M	PX = P-D+X/IRATE·M

With:

M:	Scale pitch (mm)
N:	Segment length of the reference marks at the scale (mm)
S:	Reference point step width at the scale (mm)
k:	Reference mark number at the scale
P(k):	Absolute position of the reference mark k (mm)
d:	Triggered reference mark distance (increments)
D:	Triggered reference mark distance (mm)
X:	count value (increments)
PX:	Absolute position of the sensors (mm)

11.6 Configuration of t_{pp} and f_{osz}

The GC-IP201(B) is configured by the end user in accordance to the requirements of the sensor and the subsequent electronics. See chapters 7.3 and 7.4.

Table 50: Configuration tpp

<table>
<tr><th colspan="3">ABZ output used?</th></tr>
<tr><td>No</td><td colspan="2">Yes</td></tr>
<tr><td rowspan="4">CFG1/MABZ=0
CFG1/TPP(2:0) any value
$f_{MAX} = f_{OSZ} / 90$</td><td colspan="2">CFG1/MABZ=1
Condition: $t_{pp\ (counter\ at\ ABZ)} < t_{pp\ (GC\text{-}IP201(2))}$</td></tr>
<tr><td colspan="2">Oscillator frequency specified?</td></tr>
<tr><td>No</td><td>Yes</td></tr>
<tr><td>CFG1/TPP(2:0) any value
typical: CFG1/TPP(2:0)='001'
$N = 2^{CFG1/TPP(2:0)}$

$4\ MHz \leq f_{OSZ} < N/t_{pp\ (counter\ at\ ABZ)} \leq 40\ MHz$</td><td>$N = 2^{CFG1\text{-}TPP(2:0)} > t_{pp\ (counter\ at\ ABZ)} \cdot f_{OSZ}$</td></tr>
<tr><td colspan="3">$t_{pp\ (GC\text{-}IP201(2))} = N / f_{OSZ}$
$f_{MAX} < 0.9 \cdot f_{OSZ} / (N \cdot IRATE)$ **und** $f_{MAX} < f_{OSZ} / 90$</td></tr>
</table>

Example a)

- The minimum edge interval of the electronics connected to A, B and Z is 250ns.
- The interpolation rate is 200.
- The maximum input frequency is 10 kHz.
- The oscillator frequency can be selected freely. But have to be placed in the range of 4 MHz ... 40 MHz.

CFG1/MABZ = 1 CFG1-TPP(2:0)='001' → **N = 2** $f_{OSZ} < 2/250ns$, 10kHz > $0.9 \cdot f_{OSZ} / (2 \cdot 200)$ → 4.44 MHz < f_{OSZ} < **8 MHz**	CFG1/MABZ = 1 CFG1-TPP(2:0)='010' → **N = 4** $f_{OSZ} < 4/250ns$, 10kHz > $0.9 \cdot f_{OSZ} / (4 \cdot 200)$ → 8.88 MHz < f_{OSZ} < **16 MHz**	CFG1/MABZ = 1 CFG1-TPP(2:0)='011' → **N = 8** $f_{OSZ} < 8/250ns$, 10kHz > $0.9 \cdot f_{OSZ} / (8 \cdot 200)$ → 17.77 MHz < f_{OSZ} < **32 MHz**

Example b)

- The minimum edge interval of the electronics connected to A, B and Z is 150ns.
- The interpolation rate is 160.
- The maximum input frequency is 33 kHz.
- The maximum input frequency is determined on the basis of the specified parameters.

CFG1/MABZ = 1
$N = 2^{CFG1\text{-}TPP(2:0)} > 150\ ns \cdot 33\ MHz \rightarrow N > 5$
CFG1-TPP(2:0)='011' → **N = 8**
$f_{MAX} = 0.9 \cdot 33\ MHz / (8 \cdot 160)$
f_{MAX} = 23.2 kHz

11.7 Configuration of the interfaces SPI/BiSS/SSI

The interface of the GC-IP201(B) is configured in accordance with the requirements of the interface master and the data format of the positioning data within the software. Refer to chapters 8.1, 8.2, 8.3 and 7.8.

Example a) SPI mode

- The counter value and the status information shall be read as fast as possible.
- Multi turn information is not required.
- The clock frequency of the IC is 40 MHz.

Configuration	Value	Remark
CFG2/ASYNC	1	Maximum data rate at SPI interface
CFG2/SYNC	Any value	Register `POSIT` is not used
CFGBISS/MTBIT	Any value	Register `POSIT` is not used
CFGBISS/STBIT	Any value	Register `POSIT` is not used
CFGBISS/GRAY	Any value	Register `POSIT` is not used
CFGBISS/CLK10	1	40MHz > 10MHz.
CFGBISS/READ32	Any value	BiSS interface inactive
CFGBISS/BISSTO	Any value	BiSS interface inactive
CFGBISS/RING	Any value	SSI interface inactive
CFGBISS/SSITO	Any value	SSI interface inactive

Example b) SPI mode

- All data registers are read using a software timer.
- 8 Bit Multi turn data are required.
- The internal oscillator is used.

Configuration	Value	Remark
CFG2/ASYNC	0	equidistant measuring per software timer
CFG2/SYNC	00100bin	Some Register require this value
CFGBISS/MTBIT	01bin	8 Bit multi turn data → 22 Bit single turn data
CFGBISS/STBIT	30dec	The maximum bit number is used for single turn data
CFGBISS/GRAY	0	Usually binary data will transmitted via SPI interface
CFGBISS/CLK10	1	40 MHz > 10 MHz
CFGBISS/READ32	Any value	BiSS interface inactive
CFGBISS/BISSTO	Any value	BiSS interface inactive
CFGBISS/RING	Any value	SSI interface inactive
CFGBISS/SSITO	Any value	SSI interface inactive

Example c) BiSS-C-Mode

- No multi turn data are required but maximum resolution of the single turn data
- The transmission shall happen in binary code.
- The clock frequency of the GC-IP201B is 40MHz.
- Per BiSS register access only configuration data shall be read and write.

Configuration	Value	Remark
CFG2/ASYNC	Any value	No transmission of data registers per register access
CFG2/SYNC	Any value	No transmission of data registers per register access
CFGBISS/MTBIT	00bin	0 Bit multi turn data → 32 Bit single turn data
CFGBISS/STBIT	30dec	30 Bit single turn data, two leading 0-bit added, for 32 bit value
CFGBISS/GRAY	0	Binary code
CFGBISS/CLK10	1	40 MHz > 10 MHz
CFGBISS/READ32	0	No transmission of data registers per register access
CFGBISS/BISSTO	9dec	BiSS time out = 512/40 MHz = 12.8 µs
CFGBISS/RING	Any value	SSI interface inactive
CFGBISS/SSITO	Any value	SSI interface inactive

Example d) BiSS-C-Mode

- 12 Bit multi turn data and 13 Bit single turn data required.
- The transmission shall happen in gray code.
- The clock frequency of the GC-IP201B is 8MHz.
- Per BiSS register access configuration data shall be changed and ADC values shall be read out from the IC for monitoring purposes.

Configuration	Value	Remark
CFG2/ASYNC	Any value	Any value for register ADC
CFG2/SYNC	Any value	Any value for register ADC
CFGBISS/MTBIT	10bin	12 Bit multi turn data → 20 Bit single turn data
CFGBISS/STBIT	13dec	13 Bit single turn data, 7 leading 0-bit added, for 20 bit value
CFGBISS/GRAY	1	Gray code
CFGBISS/CLK10	0	8 MHz < 10 MHz
CFGBISS/READ32	1	Transmission of data registers possible
CFGBISS/BISSTO	7dec	BiSS time out = 128 / 8 MHz = 16µs
CFGBISS/RING	Any value	SSI interface inactive
CFGBISS/SSITO	Any value	SSI interface inactive

Example e) SSI mode 13 Bit

- No multi turn data are required but maximum resolution of the single turn data
- The transmission shall happen in binary code.
- The clock frequency of the GC-IP201B is 40MHz.
- The SSI master operates in ring mode with a time 4 µs.

Configuration	Value	Remark
CFG2/ASYNC	Any value	Any value for SSI
CFG2/SYNC	Any value	Any value for SSI
CFGBISS/MTBIT	Any value	Any value for SSI 13 Bit
CFGBISS/STBIT	30dec	The maximum bit number is used for single turn data
CFGBISS/GRAY	0	Binary code
CFGBISS/CLK10	1	40 MHz > 10 MHz
CFGBISS/READ32	Any value	BiSS interface inactive
CFGBISS/BISSTO	Any value	BiSS interface inactive
CFGBISS/RING	1	Ring mode possible
CFGBISS/SSITO	157dec	SSI time out = 160 / 40 MHz = 4µs

Example f) SSI mode 25 Bit

- 8 Bit multi turn data and 12 Bit single turn data are required.
- The transmission shall happen in gray code.
- The clock frequency of the GC-IP201B is 8MHz.
- The SSI master operates in ring mode with a time 18 µs.

Configuration	Value	Remark
CFG2/ASYNC	Any value	Any value for SSI
CFG2/SYNC	Any value	Any value for SSI
CFGBISS/MTBIT	01bin	8 Bit multi turn data → 16 Bit single turn data
CFGBISS/STBIT	12dec	12 Bit single turn data, 4 leading 0-bit added, for 16 bit value
CFGBISS/GRAY	1	Gray code
CFGBISS/CLK10	0	8 MHz < 10 MHz
CFGBISS/READ32	Any value	BiSS interface inactive
CFGBISS/BISSTO	Any value	BiSS interface inactive
CFGBISS/RING	1	Ring mode possible
CFGBISS/SSITO	141dec	SSI time out = 144 / 8 MHz = 18µs

11.8 BiSS configuration file idbiss4743.xml

For automatic detection of the GC-IP201B at BiSS-C master devices, the file *idbiss4743.xml* can be used. For correct data format detection of the single cycle data (SCD) it is recommended to change the manufacturer code within the BiSS area according the EEPROM settings for the number of the multi turn bits (refer to chapter 7.8).

Table 51: Biss configuration using idbiss4347.xml

CFGBiSS/MT	Recommended manufaturer code	SCD (Pos 0)	SCD (Pos 1)	SCD (Pos 2)	SCD (Pos 3)
00bin	0x51 0x01 0x1E 0x00	2 Bit unused	30 Bit single turn	1 Bit error	1 Bit warning
01bin	0x51 0x01 0x18 0x08	8 Bit multi turn	24 Bit single turn	1 Bit error	1 Bit warning
10bin	0x51 0x01 0x14 0x0C	12 Bit multi turn	20 Bit single turn	1 Bit error	1 Bit warning
11bin	0x51 0x01 0x10 0x10	16 Bit multi turn	16 Bit single turn	1 Bit error	1 Bit warning

12 Notes