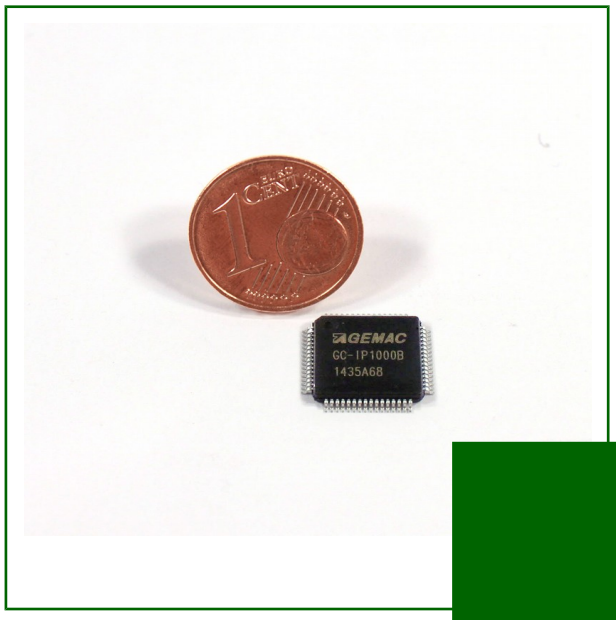
GC-IP1000B

Datasheet

Version: 2.3
Date: 18/01/2017



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Revision History

Date	Revision	Changes
10/12/2007	2.2	GC-IP1000B added
18/01/2017	2.3	change to new AMAC document layout

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1 Overview

The interpolation circuit GC-IP1000B serves to increase the resolution for incremental position and angular measuring systems with sinusoidal output signals offset by 90°. The IC divides the signal period up to 1000 times.

The GC-IP1000B comprises three instrument amplifiers with adjustable gain factors. Incremental encoders which possess a voltage interface, and measuring bridges can be connected directly. The IC may operate with both single-ended and differential input signals. The input signals are subjected to an AMAC-specific internal gain and offset control. The amplitude is controlled in the range between 80 % and 120 % of the standard amplitude. The control range for the offset of the two input signals is —10 % of the nominal amplitude. The phase displacement of the input signals can be corrected statically using a digital potentiometer.

To suppress the edge noise of the output signals at low input frequencies and at standstill a glitch filter can be activated. Thus, in case of a short-time disturbance of the input signals, a subsequent interpolation counter will operate without errors.

The IC is configured specifically to the particular application via configuration pins, an EEPROM or via the serial interface of the GC-IP1000B.

The GC-IP1000B is pin compatible to the GC-IP1000.

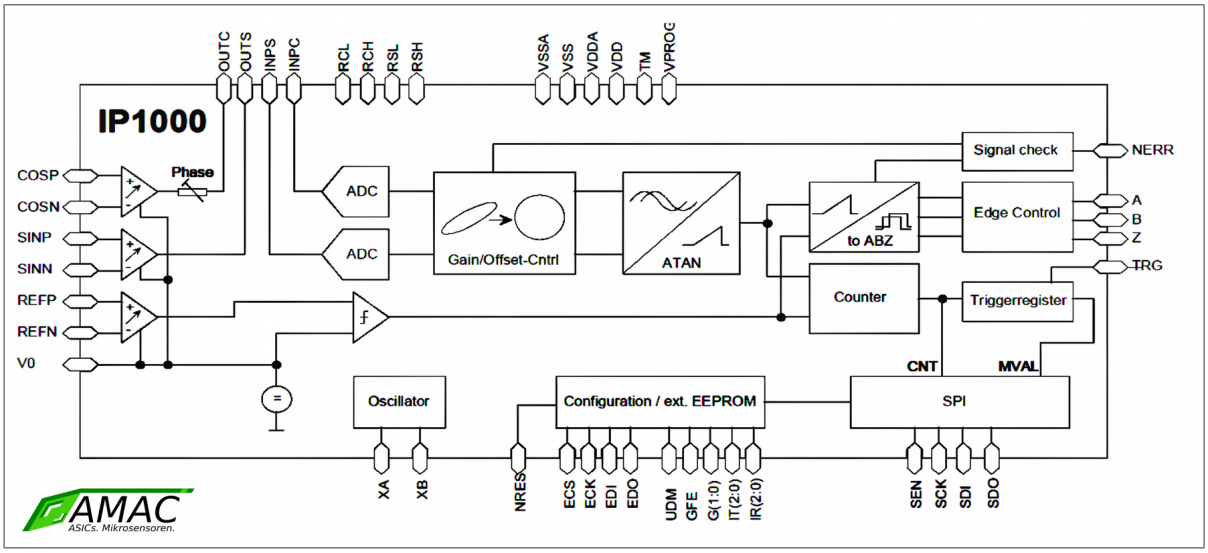


Figure 1: Blockschaltbild

2 Features

Table 1: Features

Features	
Analog input	3 channels differential: sine/cosine/reference signal Standard connection 1Vpp (differential) Input ranges: 100mVpp, 120mVpp, 145mVpp (differential) Single-ended input 2.0Vpp Input frequency of up to 110kHz
Signal correction	Automatic offset and amplitude controller Digital potentiometer for phase
Interpolation rate	1000, 800, 500, 400, 250, 200, 125, 100
Output for measuring values	28-bit counting value 90° square-wave sequences or up/down counting pulses resp. Error signal
Configuration options	Via configuration pins Via serial interface (SPI) Via EEPROM
Serial interface (SPI)	For configuration and measuring-value output 16-bit synchronous/asynchronous mode Not required for minimum configurations
EEPROM	Up to 8 configuration banks For controller settings (gain / offset / phase) In conjunction with SPI, for any user data Not required for minimum configurations
Miscellaneous	Filter for suppressing edge noise at low speeds Programmable interval time for adapting the IC to slower electronic evaluation equipment Edge-controlled measuring-value trigger Programmable response of the IC to sensor errors
Package	TQFP64 (10mm x 10mm x 1mm)

3 Pin Assignment

Table 2: Pin Assignment

Pin	Name	Type	Description
1	EDI	Digital output / COUT	EEPROM: data output
2	ECKL	Digital output / COUT	EEPROM: clock
3	SDO/RDY	Digital output / CODO	SPI-data output [6]
4	SDI	Digital input / TTLIN	SPI-data input [5]
5	SCEN	Digital input / TTLIN	SPI-enable [4]
6	SCLK	Digital input / TTLIN	SPI-clock [5]
7	TRG	Digital input / TTLIN	Trigger input [5]
8	TM	Digital input / TTLIN	Test mode [3]
9	UDMODE	Digital input / TTLIN	Output mode [5]
10	GFE	Digital input / TTLIN	Glitch-Filter-Enable [5]
11	MODE	Digital input / TTLIN	ADU-Mode [3]
12	IT2	Digital input / TTLIN	Configuration interval time [5]
13	IT1	Digital input / TTLIN	Configuration interval time [5]
14	IT0 / DP3*)	Digital input / TTLIN	Configuration interval time5) DProg 3 *)
15	IR2 / DP2*)	Digital input / TTLIN	Configuration interpolation rate [5] DProg 2 *)
16	IR1 / DP1*)	Digital input / TTLIN	Configuration interpolation rate [5] DProg 1 *)
17	IR0 / DP0*)	Digital input / TTLIN	Configuration interpolation rate [5] DProg 0 *)
18	XA/CLK	Oszillator / Digital input	Clock
19	XB	Oszillator	Clock [3]
20	A / UP	Digital output / COUT	Incremental output A
21	B / DOWN	Digital output / COUT	Incremental output B
22	OREF	Digital output / COUT	Output reference signal / Index
23	VDD2	Power	Digital power supply voltage +5V
24	VSS2	Power	Digital ground
25	NERR	Digital output / COUT	Error signal
26	NRES	Digital input	Reset [2]
27	VSS3	Power	Digital ground
28	REFN	Analog input	Input reference signal negative [7]
29	REFP	Analog input	Input reference signal positive [7]
30	RSL	Analog	Backup capacitor, ADC reference voltage
31	RSH	Analog	Backup capacitor, ADC reference voltage
32	OUTS	Analog Output	Analog output sine
33	SINN	Analog input	Input sine negative
34	SINP	Analog input	Input sine positive
35	INPS	Analog input	Input sine ADC
36	VDDA1	Power	Analog power supply voltage +5V
37	VSSA1	Power	Analog ground +5V
38	VSSA2	Power	Analog ground +5V
39	VDDA2	Power	Analog power supply voltage +5V

Pin	Name	Type	Description
40	V0	Analog Output	Reference voltage 1
41	V0S180	Analog Output	Reference voltage 2
42	V0S	Analog Output	Reference voltage 3
43	V0C	Analog Output	Reference voltage 4
44	VDDA2	Power	Analog power supply voltage +5V
45	VSSA2	Power	Analog ground +5V
46	INPC	Analog input	Input cosine ADC
47	COSN	Analog input	Input cosine negative
48	COSP	Analog input	Input cosine positive
49	OUTC	Analog Output	Analog output cosine
50	RCH	Analog	Backup capacitor, ADC reference voltage
51	RCL	Analog	Backup capacitor, ADC reference voltage
52	G0	Digital input / CINPU	Configuration gain
53	G1	Digital input / CINPD	Configuration gain
54	PROG	Power	Programming voltage
55	VSSP	Power	Programming ground
56	VSS1	Power	Digital ground
57	VDD1	Power	Digital power supply voltage +5V
58	ADCDAT	Digital input / TTLIN	ADC cosine data [5)]
59	ADSDAT	Digital input / TTLIN	ADC sine data [5)]
60	ADCLK	Digital output / COUT	ADC clock
61	ADCONV	Digital output / COUT	ADC start conversation
62	ECS	Digital output / COUT	EEPROM: enable
63	ERDY	Digital input / TTLIN	EEPROM: ready [4)]
64	EDO	Digital input / TTLIN	EEPROM: data input GC-IP1000B [5)]

[*)] DPROG pins:
- Default: IR(2:0) , IT(0)
- EEP bank address (3-bit), if EEP exists and bank enable (address 0x0F, Bit 0) set.
- HW address when the command to this effect comes from the SPI.

[2)] During power-on, no H level may be driven at NRES (use open-drain driver).
[3)] When not used: at low
[4)] When not used: at high
[5)] When not used: either at low or at high
[6)] When not used: at separate pull-up resistor.
[7)] When not used: any connection permitted, REFN and REFP should not be connected to the same potential.

ⓘ *Each IC input requires a defined connection*

4 Configuration

4.1 Reset

After a reset of the IC all registers will be initialised with default values. After that the configuration pins will be read in. Those values overwrite the default values. If a valid EEPROM is connected to the IC the EEPROMvalues will overwrite pin values. During the whole reset process the pin SDO/RDY will be held low. After that the configuration register can be changed via the serial interface SPI. For starting a new configuration in case of an error it is possible to connect the pins NRES and NERR. If they are connected, the reset signal will be held by the „NERR-chain“ until one of its flip flops come to „0“.

Table 3: Register Default Values

Name	Meaning	Default Value
IR(2:0)	Interpolation rate	Pin IR(2:0) will be read in
IT(2:0)	Interval time	Pin IR(2:0) will be read in
GFE	Glitch-filter-enable	Pin GFE will be read in
UDMODE	Output mode A/B or Up/Down	Pin UDMODE will be read in
DISREG	Disable signal regulation	0
DISREF	Disable reference point processing	0
Speed	Speed mode for internal counter	0
TRSLP	Trigger egde	0
ADU(1:0)	Type of external ADC	0 x 00
ERRMASK	Errormask register	0 x 3F
SGAIN	Gain correction sine - start value	0 x 80
SOFF	Offset correction sine - start value	0 x 00
CGAIN	Gain correction cosine - start value	0 x 80
COFF	Offset correction cosine - start value	0 x 00
PHASE	Phase correction between sine and cosine	0 x 0F
SYNC	SPI synchronisation with internal processing	0 x 00
G0/G1	Gain selection (no register)	Pin, not via EEPROM or SPI
Mode	ADC-mode (no register)	Pin, not via EEPROM or SPI

ⓘ *The use of a supervisor IC (i.e. MAX803) is recommended to secure a correct reset processing.*

4.2 Reset Process

1. Pin SDO/RDY becomes L, all the registers are initialized by entering default values.
2. Self-calibration of the ADC is carried out, with the configuration pins being loaded into the CFG0 register.
3. Check whether an EEPROM is connected (address 0x0F containing 0x46 or 0x47).
4. If necessary, the DP(2:0) programming pins are read as the EEP basic address.
5. The EEPROM is read and the registers involved are re-written.
6. Start of normal operation of the IC.
7. Pin SDO/RDY becomes H (external pull-up resistor required) .
8. The configuration registers can be changed via the SPI.

The time between a rising edge at NRES and a rising edge at SDO/RDY, i.e. the end of the reset process, totals around 58000 system pulses.

4.3 Configuration Pins

The IC can be adapted to various measurement systems and further processing electronics by using the configuration registers. All configuration possibilities can be used if the IC will be initialised via EEPROM respectively SPI interface. The most important parameters can also be adjusted via external pin configuration. The following tables show these possibilities for configuration of GC-IP1000B.

Table 4: Configuration Possibilities

Parameter	Values	Pin	Register / Bit
Interpolation rate	1000, 800, 500,400, 250, 200, 125, 100	IR2/IR1/IR0	CFG0 / IR(2:0)
Min. edge distance t_{pp}	1, 2, 4, 8, 16, 32, 64, 128	IR2/IR1/IR0	CFG0 / IT(2:0)
Reference point processing	Enable, Disable	-	CFG1 / DISREF
Nominal signal amplitude	$1V_{pp}$, $145mV_{pp}$, $120mV_{pp}$, $100mV_{pp}$	G0/G1	-
Glitch filter	Enable, Disable	GFE	CFG0 / GFE
Output signals A/B/Z	ABZ-Mode, Up-Down-Mode	UDMODE	CFG / UDMODE
Error processing	Mask	-	ERRMASK
Phase correction	± 12° , ± 6°	-	PHASE / PHRANGE, PAHSE (4:0)
Gain regulation	Pre setting / time constant / enable, disable	-	CFG0 / DISREG, SGAIN, CGAIN
Offset regulation	Pre setting / time constant / enable, disable	-	CFG0 / DISREG, SOFF, COFF
Trigger	Measured value trigger, trigger edge	TRG	CFG1 / TRSLP
SPI-Mode	Synchron, asynchron	-	SYNC / ASYNC
SPI-Hardware address	0-15	DP(3:0)	

Table 5: Configuration of Interpolation Rate

Interpolation Rate	CFG0 - IR(2:0)	Pin IR2	*Pin IR1*	*Pin IR0*
1000	100	1	0	0
800	000	0	0	0
500	101	1	0	1
400	001	0	0	1
250	110	1	1	0
200	010	0	1	0
125	111	1	1	1
100	011	0	1	1

Table 6: Configuration of Reference Point Processing

Reference Point Processing	CFG1 - DISREF
enabled	0
disabled	1

Table 7: Configuration of Signal Amplitude (Nominal Value)

Input Signal Amplitude	Pin G1	Pin G0
1 V_{pp}	VDD	VDD
145 mV_{pp}	VDD	VSS
120 mV_{pp}	VSS	VDD
100 mV_{pp}	VSS	VSS

Table 8: Configuration of Minimum Edge Distance

Min. Edge Distance t_{pp}	CFG0 - IT(2:0)	Pin IT2	Pin IT1	Pin IT0
1/f_{osc}	000	0	0	0
2/f_{osc}	001	0	0	1
4/f_{osc}	010	0	1	0
8/f_{osc}	011	0	1	1
16/f_{osc}	100	1	0	0
32/f_{osc}	101	1	0	1
64/f_{osc}	110	1	1	0
128/f_{osc}	111	1	1	1

Table 9: Configuration of Glitch Filter

***Pin* GFE**	**CFG0 - GFE**	**Glitch Filter**
VSS	0	disabled
VDD	1	enabled

5 Function

5.1 Input Amplifier

The GC-IP1000B incorporates three instrument amplifiers with adjustable gain factors. Incremental encoders with a voltage interface and measuring bridges can be connected directly. The IC operates with both single-ended and differential input signals. The amplification is identical for all signals of the sensor (sine, cosine, index/reference). To adapt the GC-IP1000B to customised sensors, the common reference voltage of the instrument amplifier is provided at pin V0.

5.1.1 Input Signals

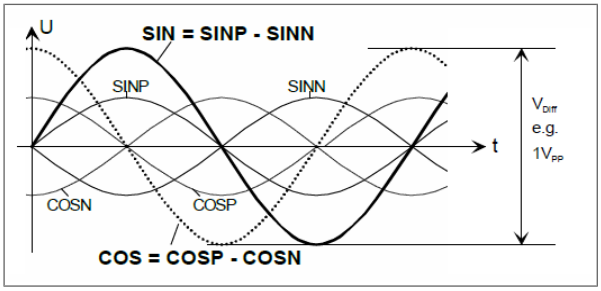


Figure 2: Input signals

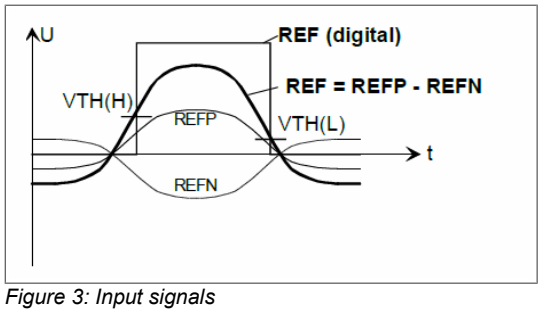


Figure 3: Input signals

Table 10: Gain Configuration

G1	L	L	H	H
G0	L	H	L	H
Gain (nominal)	19,5	16.25 [2)]	13.45	1.95
Input voltage for differential input [1)] (mV_{pp})	50	60	72	500
Input voltage U_{Diff} (nominal) (mV_{pp})	100	120	145	1000
Input voltage range for U_{diff} (mV_{pp})	80 - 120	96 - 144	145 - 174	800 - 1200
Maximum signal offset (mV_{pp})	±10	±12	±14.5	±100
Lower threshold of reference point comparator nominal VTH(L) (mV_{pp})	10	10	10	10
Upper threshold of reference point comparator nominal VTH(H) (mV_{pp})	15	15	15	15

[1)] On each of the inputs SINP, SINN, COSP, C
[2)] Default gain value with open pins G0 and G1

ⓘ *In order to achieve the maximum possible precision for amplitude and offset control, the phase potentiometer on the GC-IP1000B must be adapted to the sensor connected.*

ⓘ *In the GC-IP1000B, amplitude and offset errors are treated as one unit. In case of special application, this may mean that a larger permissible error of one parameter can be accepted if the other error becomes smaller.*

ⓘ *In case of measuring systems without a reference signal a defined status (always active or always inactive, respectively) must be set via the REFP and REFN pins.*

5.2 A/D Converter

The IC can be configured for using the internal 12-bit ADC with a maximum of 343kS/s and for the use of three different external ADC types.

Table 11: ADC Configuration

ADC	Pin Mode	CFG2 – ADU (1:0)
Internal, 12 Bit	0	any
TLC1417 (14 Bit, single-ended input)	1	00
TLC1400 (12 Bit, single-ended input)	1	01
AD7475 (12 Bit, differential / single-ended input)	1	10
Reserved	1	11

ⓘ *The use of an internal A/D converter in conjunction with the integrated analog input circuit is recommended for standard applications.*

5.2.1 Input Circuit Rating

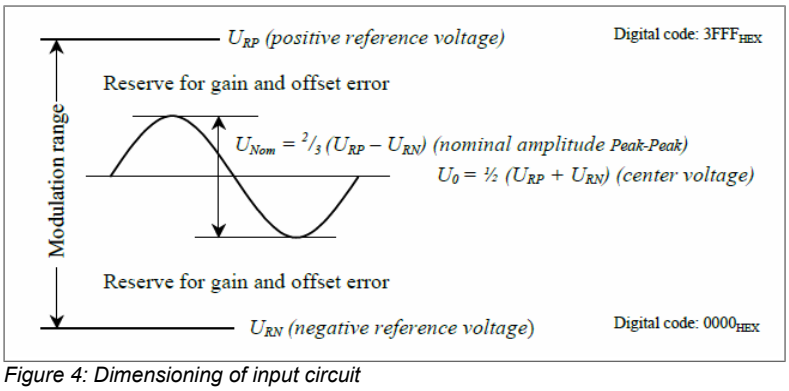


Figure 4: Dimensioning of input circuit

For the internal A/D converter, all the levels are available at IC outputs.

Table 12: ADC Configuration

	Pin	Nominal Value	Tolerances
Positive reference voltage sine	RSH	3.85 V	±100mV
Positive reference voltage cosine	RCH	3.85 V	±100mV
Negative reference voltage sine	RSL	0.70 V	±40mV
Negative reference voltage cosine	RCL	0.70 V	±40mV
voltage cosine RCL 0.70 V —40mV	V0S	2.275 V	Adjusted to internal amplifiers
Reference voltage cosine	V0C	2.275 V	Adjusted to internal amplifiers
Reference voltage for external circuits	V0	(RSH+RSL+RCH+RCL)/4	±20mV

The U0S and U0C voltages are adjusted in such a manner that the offset error of the internal amplifier can be corrected and the reference level of the amplifier is in the middle of the ADC input range.

In case of special single-ended applications, feeding directly at the integrated ADC is possible. Two sineshaped voltages with a nominal value of 2.0Vpp are required around the reference voltage at the U0. The nominal value of this reference voltage totals 2.275V and is generated from the reference voltages of the ADC.

Analog input circuits for the external converters must be designed in such a manner that the modulation reaches a level of 2/3 of the ADC maximum value at nominal input amplitude.

5.3 Interpolation

The signal periods of the analog input signals sine (SIN) and cosine (COS) are divided and provided to the serial interface (SPI) as a 28 bit count value in two's complement. The reference point can be generated via the reference signal inputs REFP and REFN or can be set via SPI. Up to two measured values can then be saved in the IC asynchronously to the access via the serial interface using a trigger input or a configurable timer. In parallel, square-wave sequences with 90° phase shift (A/B/Z signals) are generated. There are two modes which can be selected by the configuration bit UDMODE. The first mode generates the usual phase shifted square wave signals which can be count with single or 4 times evaluation. The second mode provides a up-down signal at the pins A and B.

ⓘ *Please note that the GC-IP1000B uses the digital interpolation method. This causes the speed-proportional A/B/Z output signals to be overlaid by the inevitable quantising errors (the so-called ±1INK errors) resulting from the A/D converters. When using the IC in analog closed-control loop circuits, the latter must provide an appropriate low-pass behaviour. The quantisation noise can be reduced or suppressed completely by introducing the glitch filter or activating the digital hysteresis.*

5.3.1 Interpolation Rate

Possible interpolation rates which can be selected are 1000, 800, 500, 400, 200 or 100. The term 'interpolation rate' is here understood as the number of increments into which a sinusoidal period of the input signals is divided. This corresponds to the number of signal transitions at the A/B outputs per input signal period. The number of square-wave periods at the outputs A and B amounts to . of the interpolation rate.

5.3.2 Error Signal

An error signal is generated if the input signals are no longer plausible. The error signal is also generated if the input frequency is so high that the square-wave signals are unable to follow, and/or when the maximum input frequency is exceeded. The evaluation of the internal error sources is activated via an error mask register. The response of the square-wave outputs in the event of an error can also be configured via this register. The NERR and NRES pins can be connected in order to start a re-synchronization process of the IC in the event of an error.

ⓘ *If the error signal was activated, and/or if one of the error bits was set in the result register, the present measuring result and all the following results must be discarded. Following elimination of the cause of the error and a reset of the error bit, the reference point must once again be passed by for absolute value measurements!*

5.3.3 Zero Signal Z

The zero signal Z is generated when the sine and cosine signals display a phase angle of 0° and at the same time the differential voltage of the reference inputs REFP and REFN exceeds the switching point. The switching points of the reference signal must lie in the range between 0°±[90°...180°]. The width of the zero signal Z (reference pulse) at the output is 1 increment, i.e. . period of the output signals A and B.

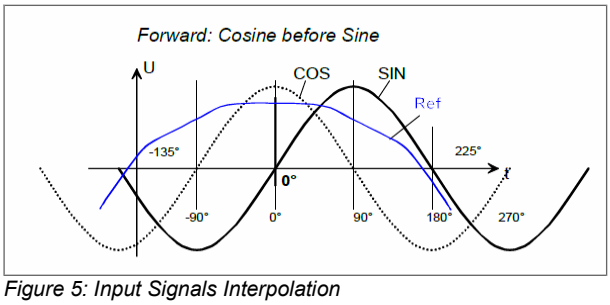


Figure 5: Input Signals Interpolation

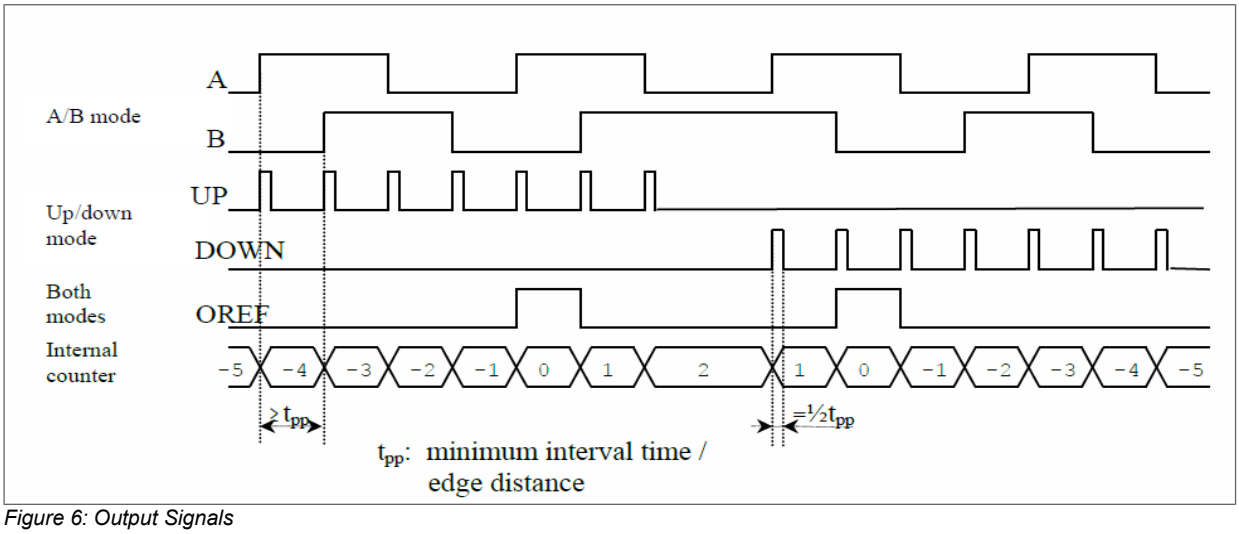


Figure 6: Output Signals

5.3.4 Maximum Input Frequency

The maximum input frequency depends on the selected interface at the output. If the square wave signals will be used as output the maximum input frequency is limited by the interpolation rate and the minimum edge distance (t_{pp}). If the internal counter is used the maximum input frequency is determined by the oscillator frequency f_{OSC} .

5.3.5 Edge Distance Control

The interval time (IT) respectively the minimum edge distance t_{pp} at the output signals can be adjusted between $1/f_{OSC}$ and $128/f_{OSC}$ in binary steps.

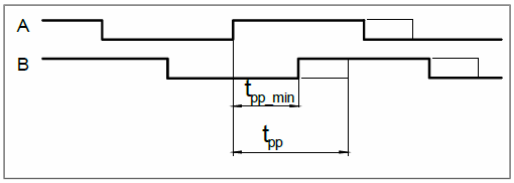


Figure 7: Edge Distance

In counter mode (the Speed bit in the Config1 register being set), the maximum input frequency totals $f_{max}=f_{osc}$ /200. In all the other modes, the maximum input frequency is limited by the minimum pulse distance at the output, where:

$f_{max} = 0.86*f_{OSC}/(IR*IT) < f_{osc}/200$
f_{osc}: frequency at pin XA
IR: activated interpolation rate
IT: activated interval time

ⓘ *These values apply on condition of an adjusted phase between the input signals and a steady state of the internal signal controller. Until this time, the input frequency must not exceed 50% of the specified maximum frequency.*

The limit values are a maximum input frequency of 110kHz with a clock frequency of 22MHz on one hand, as well as a guaranteed edge distance of 128µs at the A/B signals with a clock frequency of 1MHz on the other. Between these two values, a large number of specific systems can be adapted by selecting a suitable clock frequency and interval time of the GC-IP1000B. The requirements of the sensors as well as the further processing electronic determines the configuration of the GC-IP1000B.

5.3.6 Configuration of t_{pp} and f_{osc}

<table>
<tr><th colspan="4">Are the outputs ABZ used?</th></tr>
<tr><th>No</th><th colspan="3">Yes</th></tr>
<tr><td rowspan="4">CFG1-SPEED = 1
ERRMASK-FAST1 = 1
ERRMASK-FAST2 = 0
resp.
ERRMASK = 0xDF
CFG0-IT(2:0): no preference
$f_{MAX} = f_{OSC} / 200$</td><td colspan="3">CFG1-SPEED = 0
ERRMASK-FAST1 = 1
ERRMASK-FAST2 = 1
resp.
ERRMASK = 0x3F or 0xFF
Attention: $t_{pp\ (counter\ at\ ABZ)} < t_{pp\ (GC-IP1000B/IP501)}$</td></tr>
<tr><td colspan="3">Is the oscillator frequency prescribed?</td></tr>
<tr><td colspan="2">No</td><td>Yes</td></tr>
<tr><td>N = 2
CFG0-IT(2:0) = '001'
$f_{OSC} < 2/t_{pp\ (counter\ at\ ABZ)}$
$t_{pp\ (GC-IP1000B/IP501)} = 2/f_{OSC}$</td><td>N = 1
CFG0-IT(2:0) = '000'
$f_{OSC} < 1/t_{pp\ (counter\ at\ ABZ)}$
$t_{pp\ (GC-IP1000B/IP501)} = 1/f_{OSC}$</td><td>$N = 2^{CFG0\text{-}TPP(2:0)} > t_{pp\ (counter\ at\ ABZ)} \cdot f_{OSC}$
$t_{pp\ (IP1001)} = N/f_{OSC}$</td></tr>
<tr><td colspan="3">$f_{MAX} \approx 0.86 \cdot f_{OSC} / (N \cdot IRATE) < f_{OSC} / 200;$</td></tr>
</table>

Example:
a) The minimum edge distance of the electronic which is connected to A, B and Z is 250ns. The interpolation rate is 1000fold, the maximum input frequency will be 1kHz. The Oscillator frequency can be chosen free.

CFG1-SPEED = 0
ERRMASK-FAST1 = 1
ERRMASK-FAST2 = 1
CFG1-IT(2:0) = '001'
$f_{OSC} < 2/250$ ns, 1kHz > 0.86 · f_{OSC} / (2·1000)

→ 3MHz < f_{OSC} < 8MHz

b) The minimum edge distance of the electronic which is connected to A, B and Z is 150ns. The interpolation rate is 800fold. The oscillator frequency is 20MHz. The maximum input frequency will be determined by the prescribed parameters.

CFG1-SPEED = 0
ERRMASK-FAST1 = 1
ERRMASK-FAST2 = 1
$N = 2^{CFG1\text{-}TPP(2:0)} > 150ns \cdot 20MHz \rightarrow N > 3 \rightarrow N = 4$
→ CFG1-IT(2:0) = '010', N=4, f_{MAX} = 0.86 ·20MHz / (4·800),

→ f_{MAX} = 5.375kHz

5.4 Glitch Filter

The minimum time interval t_{pp} at which the output signals A, B and Z may switch can be adjusted in binary steps between $1/f_{OSC}$ and $128/f_{OSC}$. Furthermore, it is possible to activate a digital filter for these outputs. In this case, the minimum edge interval (t_{pp}) is changed automatically to $1024/f_{OSC}$. After switching of one of the outputs, the subsequent edge of the other signal will only be visible at the IC output after the time t_{pp} has elapsed. Thus, in case of a short-time disturbance of the input signals, a subsequent interpolation counter will operate without errors.

ⓘ *Note that in the switching range to the automatic activation / deactivation of this filter, the A/B output signals are not speed-proportional in each case.*

5.5 Measured-Value Trigger

The current count value can be loaded into the trigger hold register (SPI register TRG) with a signal edge at pin TRG. The FROZEN bit is then set in this case. Re-triggering is disabled until this bit is reset by one of the SPI commands 0x05 (CLRTRG) or 0x01 (RESCNT), respectively. Bits 31 and 30 of the trigger hold register TRG represent the state of the signal, i.e. FROZEN and TRG. The active trigger edge can be set by the configuration bit TRGSLP (register CFG1).

5.6 Error Processing

The IC has 6 sources for generating the error signal. Each source can be activated by the pertinent bit in the error mask register. With the LatchErr bit being activated, the individual error signals are stored until the next reset or until the next SPI command ResetCount (command 0x01), respectively. The logic OR function of the error signals which are masked or disabled in this way is output as an L-active signal at pin NERR. With the HoldErr bit being active, the A_UP, B_Down and Z outputs then do not change any longer in this case. The NERR and NRES pins can be connected in order to re-synchronize the IC in the event of an error. The error signal is then active for 4 system cycles in this case.

Table 13: Error Processing

Bit	Meaning	Default
GCOMP	The automatic gain controller has reached its control limit.	1
OCOMP	The automatic offset controller has reached its control limit.	1
BQLOW	Amplitude error: the vector resulting from sine and cosine is too small.	1
ADUOVL	Clipping of one of the A/D converters.	1
FAST1	Input frequency too high, direction detection is no longer possible (Config-Bit Speed = 1). Input frequency too high; A/B signals can no longer be generated (Speed = 0).	1
FAST2	Input frequency too high; square-wave signals are no longer able to follow (depending on IT(2:0)), no effect if IT(2:0) equal to 000.	1
HoldERR	Output signals are not changed in the event of an error.	0
LatchERR	The masked error signal is stored until the SPI command 0x01 or reset, respectively.	0

The five error signals which are relevant for counter mode, i.e. SENS = BQLOW or ADCOVL, GCOMP, OCOMP, and FAST , are stored in the 4 MSBs of the SPI count value (read address 0x00).

5.6.1 Sensor Breakage Error:

Partial or complete tearing off of the sensor connected is detected in the GC-IP1000B at the time of occurrence. Thereafter, the signal controller tries to compensate this error which, due to the large value range of the signal adjustment registers, can lead to a situation where the cause of this error seems to have been eliminated. Even after a reset of the IC, it may happen that not all the error conditions are identified, depending on the controller initialization values which have been configured (refer also to the application notes).

ⓘ *A value of 0x3F or 0xFF, respectively, in the error mask register is recommended for square-wave operation (A/B or UP/DOWN), whilst a value of 0xDF is recommended for counter mode with the SPEED bit being set in the CFG1 register.*

6 Serial Interface

The serial interface contains a 16-bit shift register for read accesses and write accesses each. An additional 16-bit hold register series for the intermediate storage of the two MSBs during read accesses. An 8-bit address register is used for both read and write accesses. Writing into the GC-IP1000B takes place in a byteoriented manner, reading being a word-oriented process. Transmission itself is effected as 16-bit words. A written read command triggers the pertinent data output during the next access. A single-byte command is executed at the end of data transmission. Up to 16 channels can be operated at this interface. The hardware address of the IC is determined by reading the DP(3:0) pins by a special command.

6.1 Signals

The GC-IP1000B is a slave which evaluates commands and data received, but which is unable to start a communication process. The SPI protocol is executed via 4 lines:

SDI	Data input
SDO	Data output (open drain), SDO also serving as the RDY signal
SCLK	Clock
SCEN	Enable

Each transfer process is triggered by the sending of a command. To this effect, SEN is kept at L during 16 SCLK clock cycles. The input data at SDI is evaluated a the rising edge of SCLK. At the same time, the shifting of the data of the hold register is triggered at every rising edge at SCLK.

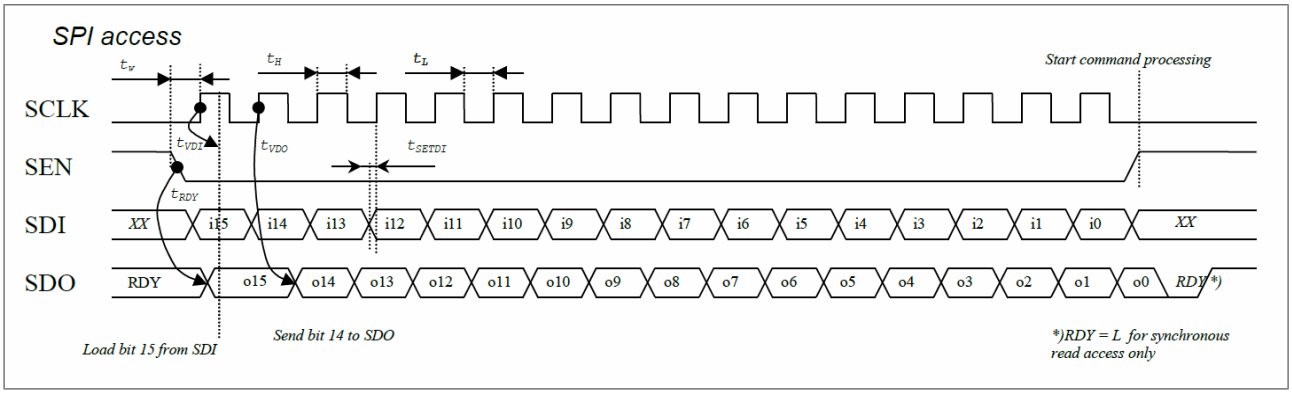


Figure 8: SPI Access

Table 14: SPI

Name	Min	Max	Meaning
t_H	2 x T_{OSZ} + 15 ns[1)]		SPI clock, H time
t_L	2 x T_{OSZ} + 15 ns[1)]		SPI clock, L time
t_w	2 x T_{OSZ} + 15 ns[1)]		Waiting time between SEN falling and SCLK rising
t_{RDY}	3 x T_{OSZ} + 15 ns	4 x T_{OSZ} + 15 ns	Switching delay RDY / SDO from SEN
t_{VDI}		15 ns	Time between SCLK rising and data read
t_{SETDI}	1 x T_{OSZ} + 15 ns[1)]		Setup time SDI before SCLK
t_{VDO}	4 T_{OSZ} + 15 ns	5 T_{OSZ} + 15 ns	Time between SCLK rising and data output

[1)] 15ns: only if clock at SCLK independent from system clock (at pin XA), otherwise: setup time before falling edge at clock XA

6.2 SPI Protocol

Table 15: Protocol SPI

Bit No. at the SDI signal															Name	Description
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	X	0	0	X	X	X	X	X	X	X	X	X	X	X	X	RES	Reserved
0	nB[2)]	0	1	H3[2)]	H2[2)]	H1[2)]	H0[2)]	A7	A6	A5	A4	A3	A2	A1	A0	WRA	Write address
0	nB[2)]	1	0	H3[2)]	H2[2)]	H1[2)]	H0[2)]	D7	D6	D5	D4	D3	D2	D1	D0	WRD	Write data
0	nB[2)]	1	1	H3[2)]	H2[2)]	H1[2)]	H0[2)]	C7	C6	C5	C4	C3	C2	C1	C0	WRC	Write command
1	nB[2)]	0	0	H3[2)]	H2[2)]	H1[2)]	H0[2)]	A7	A6	A5	A4	A3	A2	A1	A0	RD0/ST	Read byte 0 + 1 (LSB) [1)]
1	nB[2)]	0	1	H3[2)]	H2[2)]	H1[2)]	H0[2)]	X	X	X	X	X	X	X	X	RD1	Read byte 2 + 3 (MSB)
1	nB[2)]	1	X	H3[2)]	H2[2)]	H1[2)]	H0[2)]	X	X	X	X	X	X	X	X	NOP	Output read register

[1)] This command loads the internal data into a 32-bit hold register
[2)] These bits must be set at '0' in single-channel systems

Bit	Name	Description	
nB	Broadcast (L-active)	0:	Command to all channels
		1:	Command to the channel addressed in H(3:0)
H(3:0)	Hardware address	Channel address of data transmission (for WRA/WRD/WRC only) Default: 0x00 No evaluation of nB = 0	
A(7:0)	Register address	Address within a channel	
C(7:0)	Command	Single-word command	
D(7:0)	Data word	Data to be written / data read appears at SDO	

Command word examples

Set address register in all channels connected at 0x01:	0x1001
Write data 0x48 in channel 0x04:	0x6448
Read L word from register 0x07, one IC existing only:	0x8007
Configuration of the hardware address in all the channels connected	0x3000

6.3 Synchronous / Asynchronous Mode

Read data is loaded into the hold register by the RD0/ST command. This takes place when the internal cycle counter and the SYNC register have the same contents (synchronous mode) or when the ASYNC bit is set (asynchronous mode). Pin SDO is low during the waiting time (meaning: RDY) .

With the SPI working in synchronous mode, the output data can be assigned to a sample time. Equidistant measurement is possible (refer also to the application example). Higher transmission rates are achieved in asynchronous mode.

Example: 32-bit read access synchronous with internal cycle counter

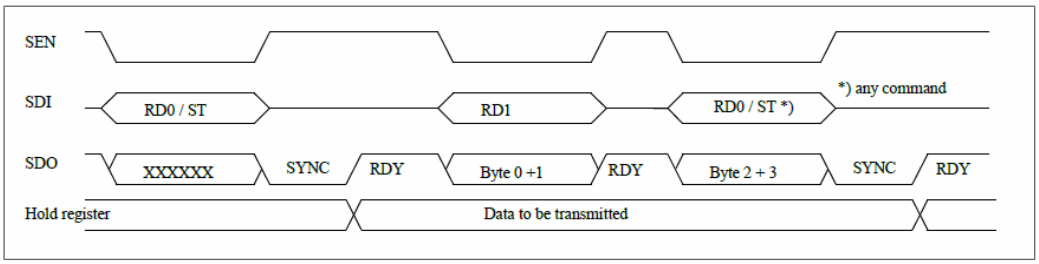


Figure 9: SPI Access

Example: 16-bit read access, asynchronous, 3 channels

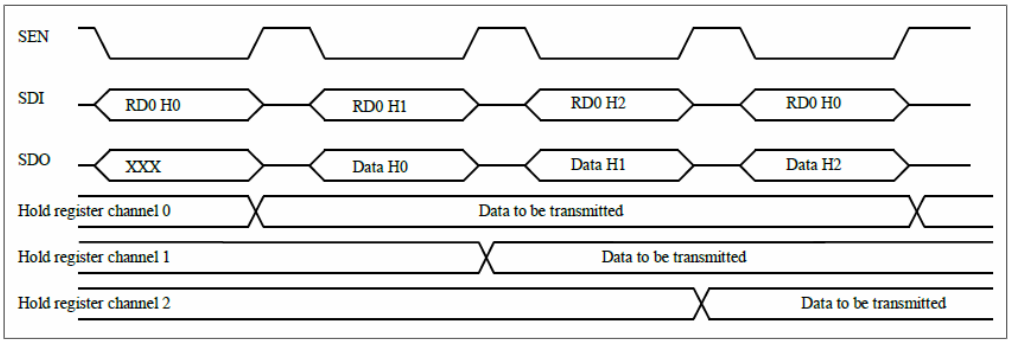


Figure 10: Read Access

Example: write access, 1 channel

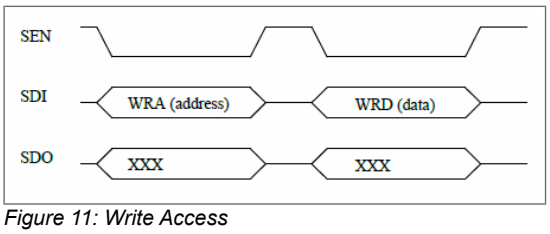


Figure 11: Write Access

Example: command execution, 1 channel

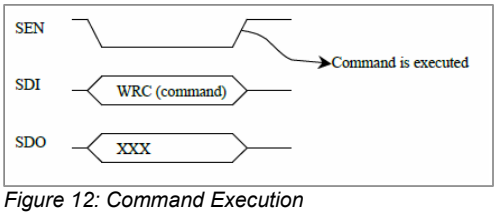


Figure 12: Command Execution

7 EEPROM

All the configuration data and controller values can be stored in an EEPROM. If this EEPROM is not connected, the IC works with the values set at the configuration pins. Following a reset (hardware, software), a check is performed in order to determine whether the EEPROM is connected, whereupon its values are read as required. Up to 8 banks of configuration data can be stored in the EEPROM.

Writing into the EEPROM always takes place via the SPI interface. This is why operation of the GC-IP1000B with SPI is once necessary for adjustment to special measuring systems and transducers.

7.1 Signals / Hardware Protocol

The ATMEL-EEPROM AT59C11 and AT93C56 types can be used in 8-bit mode. The AT93C56 requires the ERDY pin to be connected to DVDD via a pull-up resistor. Furthermore, a waiting time of > 10ms must be adhered to after every write access (WRITE / ERAL / WRAL).

7.2 Address Assignment

The addresses A6, A5 and A4 are the basic addresses for a block of configuration data. The addresses within the block correspond to the SPI write addresses. A block has a structure as follows:

Table 16: Address Assignment EEPROM

A (3:0)	Contents	A (3:0)	Contents
0	Config 0	8	Sine offset
1	Config 1	9	Cosine gain
2	Config 2	A	Cosine offset
3	ErrMask	B	Reserved (0x00)
4	Phase	C	Reserved (0x00)
5	Reserved (0x00)	D	Reserved (0x00)
6	Reserved (0x00)	E	Reserved (0x00)
7	Sine gain	F	Signature

Signature:

0x46	The data in configuration block 0 is used for configuration purposes. Blocks 1-7 can be programmed by the user with any data.
0x47	Data in the configuration block addressed by DP(2:0) are used.
sonst	The EEPROM is not used and can be programmed by the user with any data.

7.3 OP Codes

Table 17: OP Codes

EEPROM Command	Meaning	SPI Register OPC(3:0)
EWEN	Enable write commands	0011 (0x03)
EWDS	Disable write commands	0000 (0x00)
READ	Read EEPROM	1000 (0x08)
WRITE	Write EEPROM	0100 (0x04)
WRAL	Write all cells	0001 (0x01)
ERAL	Erase all cells	0010 (0x02)

8 Register

The GC-IP1000B contains 16-bit and 32-bit read registers, as well as 8-bit write registers. The addresses are assigned separately for the read and write registers. A third address area is reserved for commands.

8.1 Read Register

Table 18: Read Register

Address	Meaning	Byte 3	Byte 2	Byte 1	Byte 0
0x00	Count value / status	CNT			
0x02	Controller, sine			SOFF	SGAIN
0x03	Controller, cosine			COFF	CGAIN
0x04	EEPROM			EEPSTAT	EEPRDAT
0x05	Configuration			CFG1	CFG0
0x06	Configuration			ERRMASK	CFG2
0x07	SPI mode			DPIN	SYNC
0x09	Interpolation register	DPHI		PHI	
0x0F	Trigger	TRG			

8.2 Write Register

Table 19: Write Register

Address	Meaning	Name
0x00	Configuration	CFG0
0x01	Configuration	CFG1
0x02	Configuration	CFG2
0x03	Configuration	ERRMASK
0x04	Phase potentiometer	PHASE
0x05	Reserved	ZZ1
0x06	Reserved	ZZ2
0x07	Controller, sine (gain)	SGAIN
0x08	Controller, cosine (offset)	SOFF
0x09	Controller, sine (gain)	CGAIN
0x0A	Controller, cosine (offset)	COFF
0x0B	SPI synchronization	SYNC
0x0C	EEPROM write data	EEPWDAT
0x0D	EEPROM address	EEPADR
0x0E	EEPROM OPCode	EEPOPC

8.3 Commands

Command	Name	Description
0x00	Channel	The hardware address is read from the DP(3:0) pins. This command must always be executed as a broadcast command.. In multi-channel systems, this command must be executed as the first command after a global reset!
0x01	Reset Count	The parallel counter is reset, the error register is reset, the trigger hold register is enabled for a new trigger process.
0x02	Init	The configuration is read from the EEPROM, the parallel counter is reset, error registers are reset.
0x03	Init Control	The controller values are read from the EEPROM.
0x04	Reset Control	The automatic controllers are reset.
0x05	Clear Frozen	The trigger hold register is enabled for a new trigger process.

8.4 Coding

CNT	Status / Count value

Read address: 0x00
Reset value: 0x00

31	30	29	28	27:0
GCOMP	OCOMP	SENS	FAST1	CNT

CNT Count value (two's complement)
FAST1 Speed error
SENS Sensor error (ADC overflow or sensor breakage)
OCOMP Offset error
GCOMP Gain error

TRG	Trigger hold register status / Count value

Read address: 0x0F
Reset value: 0x00

31	30	29	28	27:0
FROZEN	TRGIN	0	0	CNT

CNT Count value (two's complement), stored in the trigger hold register
FROZEN New trigger value was stored, trigger input disabled
TRGIN Current level at the TRG pin

PHI	Interpolation result / Phase angle

Read address: 0x09 (Byte 1/0)

15:10	9:0
0x00	PHI

PHI Signal phase (unsigned binary)
Scaling: 0 ... IR = 0° ... 360°

For IRATE 1000/500/250/125 Scaling: 0...1000 = 0...360°, maximum value 999
For IRATE 800/400/200/100 Scaling: 0... 800 = 0...360°, maximum value 799

DPHI	Interpolation result / Change in phase angle

Read address: 0x09 (Byte 3/2)

15:10	9:0
0x00	DPHI

DPHI change in phase angle (two's complement)
Scaling: -IR/2 ... +IR/2 = -180° ... +180°

DPIN	DP inputs

Read address: 0x07 (Byte 1)
Reset value: Pins (DP 3:0)

7:4	3:0
0000	DP (3:0)

DP (3:0) Level at the GC-IP1000B pins DP (3:0)

CFG0	Configuration register 0

Read address: 0x05 (Byte 0)
Write address: 0x00
EEPROM-address 0x00
Reset value: Configuration pin will be read

7	6	5:3	2:0
UDMODE	GFE	IT(2:0)	IR(2:0)

IR (2:0)	Interpolation Rate	Square Wave Periods A/B
000	800	200
001	400	100
010	200	50
011	100	25
100	1000	250
101	500	125
110	250	62.5
111	125	31.25

IT (2:0)	Interval Time t_{pp} in 1/ f_{OSZ}
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

UDMODE 0 Pin A_UP and B_DOWN working in A/B-Mode
1 Pin A_UP and B_DOWN working in Up/Down-Mode

GFE 0 Glitch filter disabled
1 Glitch filter enabled

CFG1	Configuration Register 1

Read address: 0x05 (Byte 1)
Write address: 0x01
EEPROM-address 0x01
Reset value: 0x00

7:5	4	3	2	1	0
000*)	TRSLP	SPEED	DISREG	DISREF	0*)

*) *Bits must remain unchanged in order to guarantee the correct functioning of the IC*

DISREG	0	Internal signal regulation enabled
	1	Internal signal regulation disabled
TRSLP	0	Falling trigger edge at pin TRG
	1	Rising trigger edge at pin TRG
DISREF	0	Reference point processing enabled
	1	Reference point processing disabled
SPEED	0	Configure speed monitoring for A/B outputs
	1	Configure speed monitoring for internal counter

CFG2 — Configuration Register 2

Read address: 0x06 (Byte 0)
Write address: 0x02
EEPROM-address 0x02
Reset value: 0x3C

7:6	5:2	1:0
00*)	1111*)	ADU

*) *Bits must remain unchanged in order to guarantee the correct functioning of the IC*

Pin MODE	Config-Bit ADU(1:0)	ADC
L	any	internal, 12 Bit
H	0 0	TLC1417
H	0 1	TLC1400
H	1 0	AD7475
H	1 1	reserved

ERRMASK — Error Mask Register

Read address: 0x06 (Byte 1)
Write address: 0x03
EEPROM-address 0x03
Reset value: 0x3F

7	6	5	4	3	2	1	0
Latch	Hold	Fast2	Fast1	ADUOVL	BQLO	OCOMP	GCOMP

GCOMP	Enable gain error detection
OCOMP	Enable offset error detection
BQLOW	Enable sensor breakage detection
ADCOVL	Enable ADC clipping detection
FAST1	Enable speed monitoring (counter and A/B signal)
FAST2	Enable speed monitoring (A/B signal)
HOLD	Deactivate square-wave outputs in the event of an error
LATCH	Store error states

ⓘ *A value of 0x3F or 0xFF, respectively, in the error mask register is recommended for square-wave operation (A/B or UP/DOWN), whilst a value of 0xDF is recommended for counter mode with the SPEED bit being set in the Congfig1 register.*

SYNC	SPI Synchronisation Register

Read address: 0x07 (Byte 0)
Write address: 0x0B
EEPROM-address 0x0B
Reset value: 0x00

7	6	5:0
ASYNC	0	SYNCVAL

ASYNC 0 Import read data with SPI-RD0/ST the next time the contents of the cycle counter and SYNCVAL are identical
1 Import read data always with SPI-RD0/ST

SYNCVAL SPI synchronisation clock

PHASE	Phase Potentiometer

Write address: 0x04
EEPROM-address 0x04
Reset value: 0x0F

7:6	5	4:0
00	PHRANGE	PHASE

PHRANGE 0 Setting range phase potentiometer ±6°
1 Setting range phase potentiometer ±12°

PHASE 0x00 maximum phase correction negative
0x0F no phase correction
0x1E maximum phase correction positive
0x1F no phase correction

ZZ1 ZZ2	reserved reserved

Write addresses: 0x05 / 0x06
EEPROM-addresses 0x05 / 0x06
Reset value: 0x00

7:0
00000000

All the bits of these registers must be set at the value of 0.

SGAIN CGAIN	Gain correction value, sine Gain correction value,, cosine

Read addresses: 0x02 / 0x03 (Byte 0)
Write addresses: 0x07 / 0x09
EEPROM-addresses 0x07 / 0x09
Reset value: 0x80

7:0
GAIN

GAIN Current value of the gain correction register (unsigned binary)
Scaling: 0x00 Factor 0.5
0x80 Factor 1
0xFF Factor 1.5

SOFF	Offset correction value, sine
COFF	Offset correction value, cosine

Read addresses: 0x02 / 0x03 (Byte 1)
Write addresses: 0x08 / 0x0A
EEPROM-addresses 0x08 / 0x0A
Reset value: 0x00

7:0
OFFSET

OFFSET Current value of the gain correction register (two's complement)
Scaling: 0x80 maximum offset negative (-25% ADC maximum)
0x00 no offset
0x7F maximum offset positive (+25% ADC maximum)

ⓘ *Write accesses to the SOFF/COFF/SGAIN/CGAIN register serve for pre-setting - these registers are permanently updated by the internal signal controller. The scaling factor indicated applies to the behavior of the adjustment register; it does not describe the maximum signal error possible.*

EEPRDAT	EEPROM – Data read
EEPWDAT	EEPROM – Data to be written

Read address: 0x04 (Byte 0)
Write address: 0x0C
Reset value: 0x00

7:0
DATA

DATA EEPROM-Data

EEPSTAT	EEPROM – Status

Read address: 0x04 (Byte 1)
Reset value: detected EEPROM

7:3	2	1	0
0x00	EEPConf	EEPexist	EEPisBank

EEPisBank Bank-addressed EEPROM was detected
EEPexist Valid EEPROM was detected
EEPConf GC-IP1000B accesses the EEPROM for the configuration; SPI commands for configuration and/or for EEPROM access are forbidden.

EEPADR	EEPROM – Address

Write address: 0x0D
Reset value: 0x00

7	6:4	3:0
0	BANK	ADR

BANK Selection of EEPROM configuration bank
ADR Selection of EEPROM address

EEPOPC	EEPROM – instruction execution

Write address: 0x0E
Reset value: 0x00

7:4	3:0
0000	OPC

EEPROM command	Meaning	OPC(3:0)
EWEN	Enable write commands	0011 (0x03)
EWDS	Disable write commands	0000 (0x00)
READ	Read EEPROM	1000 (0x08)
WRITE	Write EEPROM	0100 (0x04)
WRAL	Write all cells	0001 (0x01)
ERAL	Erase all cells	0010 (0x02)

ⓘ *Writing to register EEPOPC triggers the start of an EEPROM access. EEPROM data is evaluated with the WRITE and WRAL OPCodes only. An EEPROM access is ignored at times when an EEP access is already active. Following execution of an EEPROM command, the SPI write registers EEPWDAT, EEPADR and EEPOPC are undefined.*

9 Signal Propagation Time

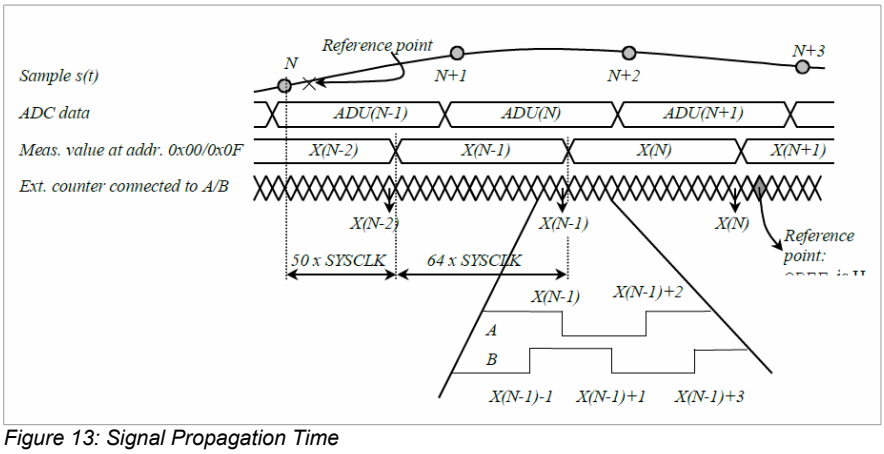


Figure 13: Signal Propagation Time

The delay time between sample time and measuring results totals 114 system cycles for the measuring value in the SPI register CNT or TRG, respectively. If a counter is used at outputs A_UP and B_Down, this time totals 178 system cycles.

ⓘ *Note that the constant delay time of the IC (as with any other digital system) means that a frequency-dependent phase offset occurs between the analog input signals and the output signals (dj = 2p·f·t_v).*

10 Parameter

Tabelle 20: Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
Operating voltage, analog / digital	4.75	5.0	5.25	V
Power consumption, analog (@20°C)	25	35	60	mA
Power consumption, digital (@20MHz & 20°C)		25		mA
Cycle low time / high time	23*)		500	ns
Oscillator at XA (external clock)				
Operating temperature	-20		85	°C
Clock frequency	1		22	MHz
Quartz at XA and XB				
Operating temperature	0		85	°C
Clock frequency	1		20*)	MHz
Internal capacitance at XA and XB		3		pF

*) If a quartz is used for the clock pulse supply, the minimum cycle of low/high time must be maintained throughout the entire temperature range.

Tabelle 21: Analog Input Part

Parameter	Min.	Typ.	Max.	Unit
Input frequency, analog part (< 1dB attenuation)			150	kHz
Phase offset between SIN and COS @100kHz		< 0.3	< 0.5	°
Amplitude SINN ⇔ SINP / COSN ⇔ COSP	80% nominal	depending on G0/G1	120% nominal	
Common-mode level SINN ⇔ SINP / COSN ⇔ COSP	1.5	V_{cc} / 2	V_{cc} – 1.5V	V
CMRR (< 5Hz)		62		dB
PSRR (< 5Hz)		62		dB
Input impedance		1GΩ||10pF		
Output current at U0S / U0S180 / U0C			100	µA
Phase adjustment (range 1)	±5	±6	±7	°
Phase adjustment (range 2)	±11	±12	±13	°
Switching range of reference point comparator		-10/+15		mV

Tabelle 22: ADC

Parameter	Min.	Typ.	Max.	Unit
Input impedance		100MW||45pF		
Reference voltage, positive (RxH)	3.75	3.85	3.95	V
Reference voltage, positive (RxL)	0.66	0.70	0.74	V
Signal amplitude (direct supply)		1.95		V_{pp}

Tabelle 23: Interpolation

Parameter	Min.	Typ.	Max.	Unit
Input frequency	0		f_{osz} / 200	kHz
Amplitude control		±20%		related to nominal
Offset control		±10%		
Interpolation rate	100		1000	
Minimum interval time A/B – signal	1 / f_{osz}		128 / f_{osz}	ns
Puls width UP/DOWN-signal	1 / (2*f_{osz})		64 / f_{osz}	ns
Interpolation accuracy		±0.7	±1.5	Ink.
Delay time (parallel counter)		114		SYSCLK
Delay time (square wave outputs)		178		SYSCLK
Puls width trigger signal an TRG	1 / f_{osz} + 15			ns

Tabelle 24: Interpolation

Parameter	Min.	Typ.	Max.	Unit
ESD immunity			1	kV
Setup-Time NRES before XA (falling edge)			15	ns

11 Package

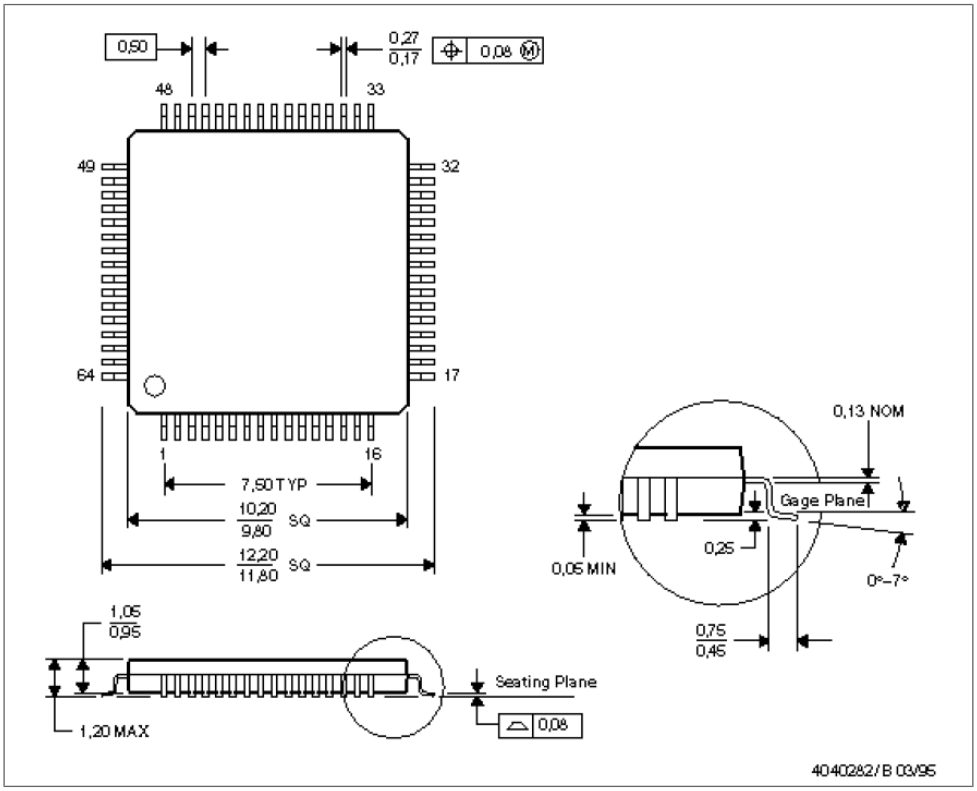


Figure 14: GC-IP1000B Package Dimensions

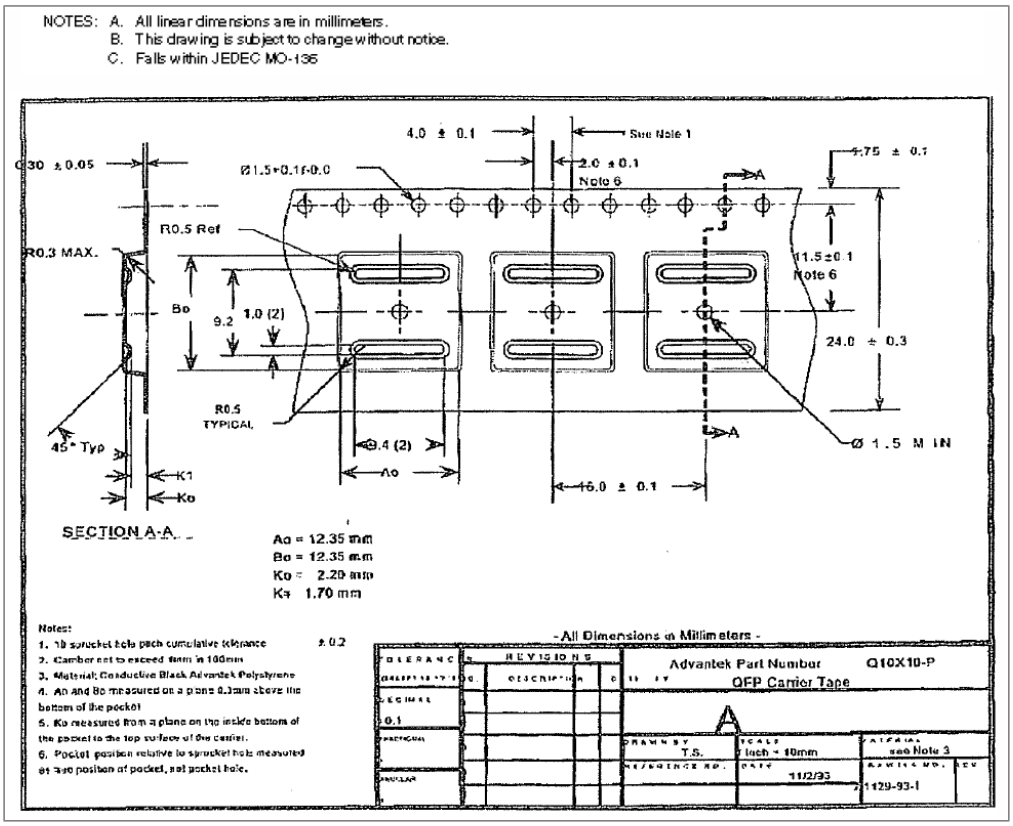
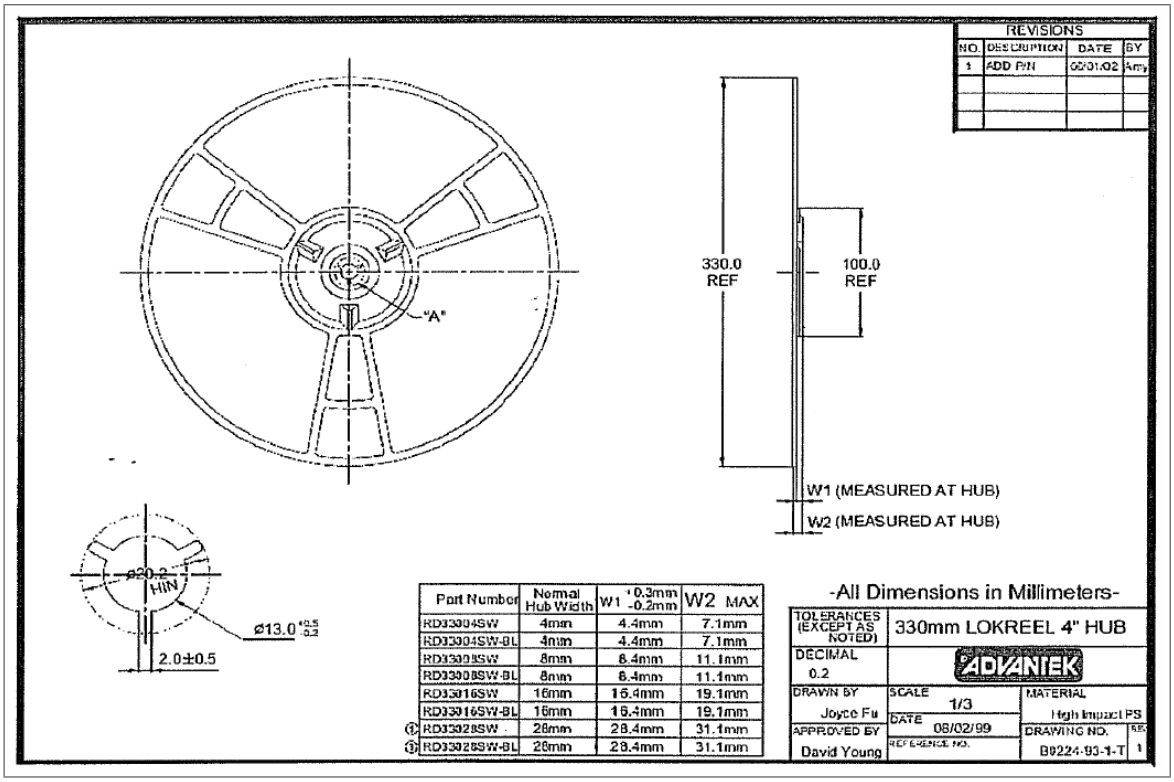


Figure 15: GC-IP1000B Carrier Tape



Part Number	Normal Hub Width	W1 +0.3mm -0.2mm	W2 MAX
RD33004SW	4mm	4.4mm	7.1mm
RD33004SW-BL	4mm	4.4mm	7.1mm
RD33008SW	8mm	8.4mm	11.1mm
RD33008SW-BL	8mm	8.4mm	11.1mm
RD33016SW	16mm	16.4mm	19.1mm
RD33016SW-BL	16mm	16.4mm	19.1mm
② RD33028SW	28mm	28.4mm	31.1mm
③ RD33028SW-BL	28mm	28.4mm	31.1mm

Figure 16: GC-IP1000B Antistatic Plastic Reel

12 Notes