AIP40

Datasheet

Version: 1.5
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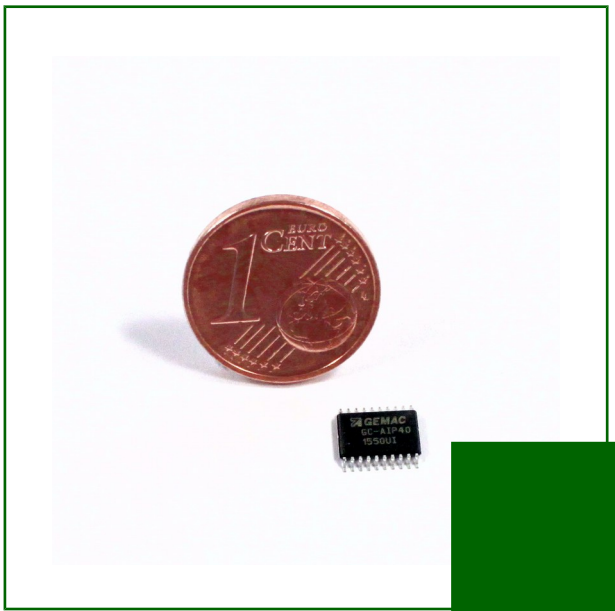

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Revision History

Date	Revision	Changes
07.12.05	1.00	Data Sheet
19.12.05	1.10	RoHS Version
10.02.06	1.20	Update
19.09.06	1.30	Update Application Notes
25.01.11	1.40	Change Boundaries of V(V0)
26/01/17	1.5	change to new AMAC document layout

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1 Overview

The Interpolation IC AIP40 is suitable for increasing the resolution of incremental position and angular measuring systems with sine shaped output signals. The IC can be used with the standard voltage signals as well as current signals. Furthermore photo diode arrays and sensor bridges can be connected directly. An adjustable minimum A/B-edge distance at the output and a programmable analogue and digital hysteresis enables also the use in case of noisy input signals.

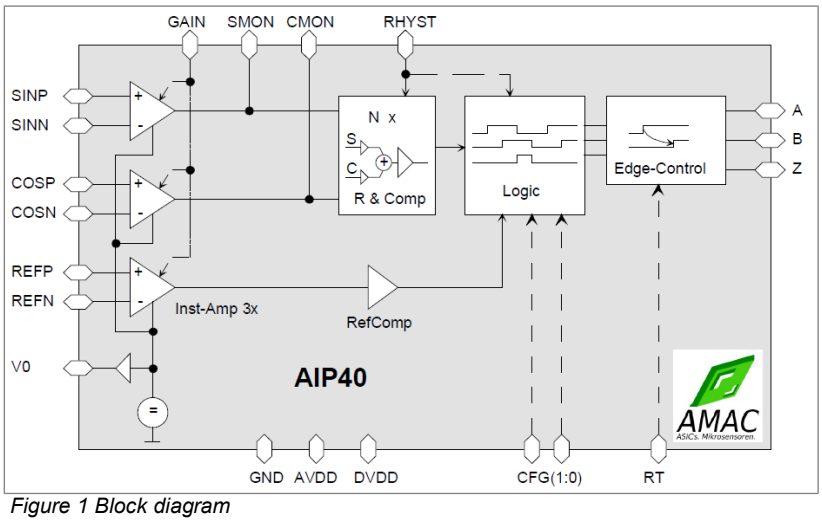


Figure 1 Block diagram

2 Features

Features	
Input signals	Sine- / cosine- / reference Signal Differential / single-ended Adjustable Gain for $1V_{pp}$ / $660mV_{pp}$ / $530mV_{pp}$ / $80mV_{pp}$
Output signals	90°-square wave (A/B/Z); TTL- and CMOS-compatible
Interpolation rate	40 / 32 / 20 / 16 / 8 / 4 edges per sine period
Input frequency	Maximum 1.2MHz for interpolation rates ≤ 20 Maximum 750kHz for interpolation rate = 32 Maximum 600kHz for interpolation rate = 40
Noise suppression	Adjustable hysteresis analogue Adjustable hysteresis digital Adjustable minimum edge distance at the output
Reference signal processing	Adjustable reference signal width at the output
Package	TSSOP20 - 4.4mm, Pitch 0.65

3 Ordering Information

Product Type	Description	Article Number
GC-AIP40	Interpolation circuit GC-AIP40, TSSOP20, RoHS conform	PR-43800-50

4 Pinning

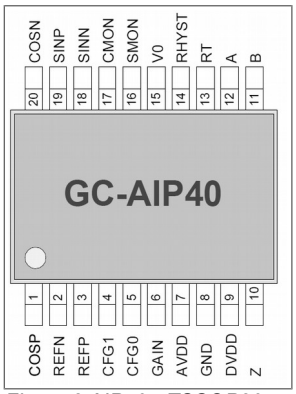
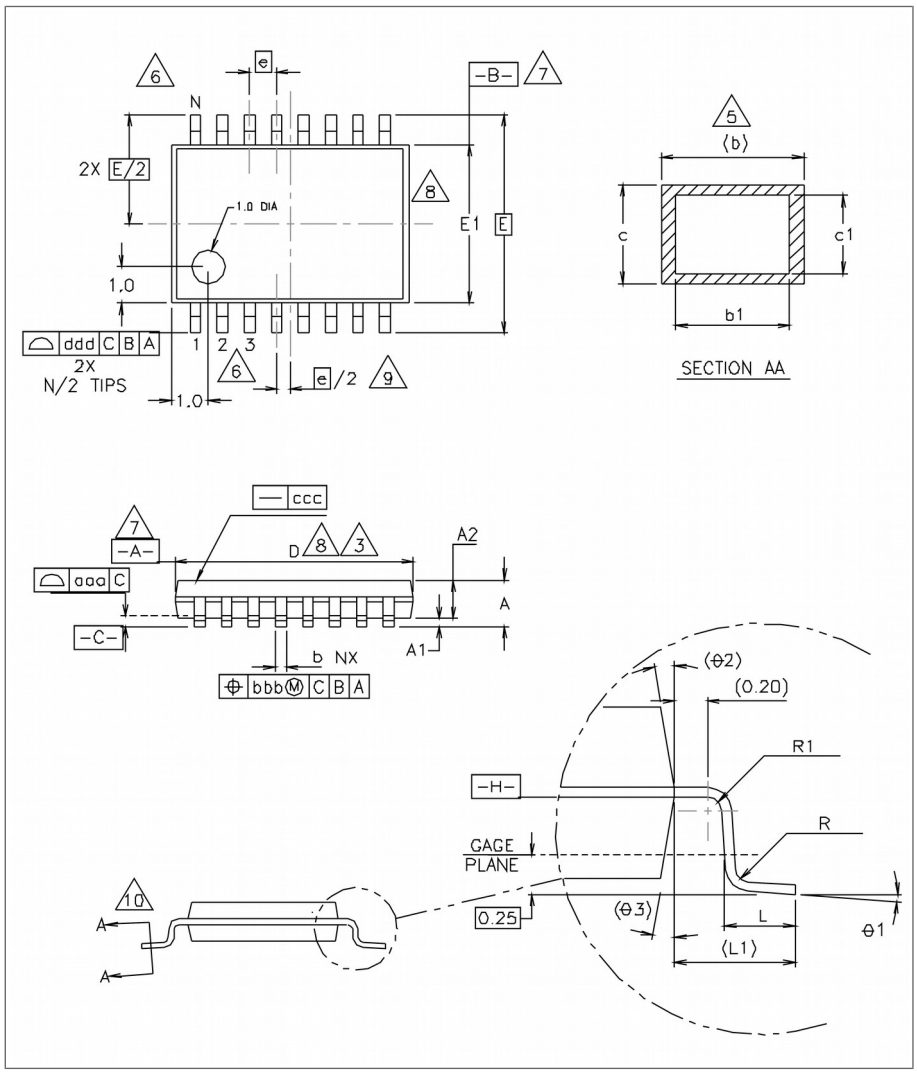


Figure 2 AIP40 - TSSOP20

Table 1 Pinning

Pin	Name	Type	Meaning
1	COSP	Input analogue	Input cosine positive
2	REFN	Input analogue	Input reference signal negative
3	REFP	Input analogue	Input reference signal positive
4	CFG1	Configuration digital (4-state)	Configuration of the interpolation
5	CFG0	Configuration digital (4-state)	Configuration of the interpolation
6	GAIN	Configuration digital (4-state)	Gain adjustment
7	AVDD	Power	Supply voltage +5V analogue
8	GND	Power	Ground analogue and digital
9	DVDD	Power	Supply voltage +5V digital
10	Z	Output digital	Output reference signal (index)
11	B	Output digital	Incremental output B
12	A	Output digital	Incremental output A
13	RT	Configuration analogue/digital	Configuration of the minimum A/B-edge distance
14	RHYST	Configuration analogue/digital	Configuration of analogue and digital hysteresis
15	V0	Output analogue	Reference voltage 2.25V
16	SMON	Output analogue	Monitoring signal sine
17	CMON	Output analogue	Monitoring signal cosine
18	SINN	Input analogue	Input sine negative
19	SINP	Input analogue	Input sine positive
20	COSN	Input analogue	Input cosine negative

4.1 Package



	MIN	NOM	MAX	Notes
D	6.40	6.50	6.60	*3,8*
E1	4.30	4.40	4.50	*4,8*
E		6.4 BSC		
e		0.65 BSC		
N		20		*6*
A			1.10	
A1	0.05		0.15	
A2	0.85	0.90	0.95	
L	0.50	0.60	0.75	
R	0.09			
R1	0.09			
b	0.19		0.30	*5*
b1	0.19	0.22	0.25	
c	0.09		0.20	
c1	0.09		0.16	
θ1	0°		8°	
L1		1.0 REF		
aaa		0.10		
bbb		0.10		
ccc		0.05		
ddd		0.20		
θ2		12° REF		
θ3		12° REF		
all				*1,2*

Figure 3 Package

Notes:

1 All dimensions are in millimeters (angles in dedrees)
2 Dimensioning and tolerancing per asme Y14.5M – 1994
3 Dimension 'D' does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
4 Dimension 'E1' does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
5 Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the 'b' dimension at maximum material condition. Dambar can not be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm for 0.5 mm pitch packages.
6 Terminal numbers are shown for reference only.
7 Datums -A- and -B- to be determined at datum plane -H-.
8 Dimensions 'D' and 'E1' are to be determined at datum plane -H-.
9 This dimension applies only to variations with an even number of leads per side, the „center“ lead must be coincident with the package centerline, datum A.
10 Cross section A-A to be determined at 0.10 to 0.25 mm from the leadtip.
11 This variation is not registered with JEDEC.

RoHS COMPLIANT 2002/95/EC

5 Configuration

Table 2 Configuration interpolation

CFG1	CFG0	IRATE	Number of square wave periods	Output Z	Input frequency
GND	GND	40-fold	10 periods	1 increment	≤ 600kHz
GND	AVDD	32-fold	8 periods	1 increment	≤ 750kHz
GND	V0	20-fold	5 periods	1 increment	≤ 1200kHz
GND	Open	16-fold	4 periods	1 increment	≤ 1200kHz
AVDD	GND	40-fold	10 periods	4 increments	≤ 600kHz
AVDD	AVDD	32-fold	8 periods	4 increments	≤ 750kHz
AVDD	V0	20-fold	5 periods	4 increments	≤ 1200kHz
AVDD	Open	16-fold	4 periods	4 increments	≤ 1200kHz
V0	GND	8-fold	2 periods	1 increment	≤ 1200kHz
V0	AVDD	4-fold	1 period	1 increment	≤ 1200kHz
V0	V0	Reserved			
V0	Open	Reserved			
Open	GND	8-fold	2 periods	4 increments	≤ 1200kHz
Open	AVDD	4-fold	1 period	4 increments	≤ 1200kHz
Open	V0	Reserved			
Open	Open	Reserved			

ⓘ *The interpolation rate (IRATE) is the number of increments in which the period of the input signals is split. These are the number of edges at the output signals A and B. The number of square wave periods at these outputs is ¼ of the interpolation rate.*

Table 3 Configuration input amplifier

GAIN	Amplitude		
	Minimum	Nominal	Maximum
GND	$0.6V_{pp}$	$1.0V_{pp}$	$1.2V_{pp}$
AVDD	$400mV_{pp}$	$666mV_{pp}$	$800mV_{pp}$
V0	$320mV_{pp}$	$530mV_{pp}$	$640mV_{pp}$
Open	$50mV_{pp}$	$80mV_{pp}$	$100mV_{pp}$

Table 4 Configuration hysteresis

RHYST	Hysteresis analogue	Hysteresis digital
Resistor R to GND	U_{Hyst} = f(R)	Deactivated
Resistor R to AVDD	U_{Hyst} = f(R)	1/40 sine period (IRATE = 40/20) 1/32 sine period (IRATE = 32/16/8/4)

Table 5 Configuration edge distance

RT	Minimum A/B-edge distance tpp		
	Minimum	Nominal	Maximum
Resistor R to GND	25ns	T_{pp} = f(R)	1700ns
Resistor R to AVDD (Mode TPP30)	26ns	33ns	40ns

6 Functional Description

6.1 Input Amplifier

The AIP40 includes three instrumentation amplifiers with adjustable gain factors. Sensors with voltage output signals as well as measuring bridges can be connected directly. Current sensors can be adapted via a simple circuit. The IC is able to process single-ended as well as differential signals. The gain setting happens using the pin GAIN, which is connected to GND, DVDD, V0 or is left open. The chosen gain is identic for all signals of the sensor (sine, cosine, index/reference). To adapt the AIP40 to specific sensors the reference voltage of the instrumentation amplifier is provided at pin V0.

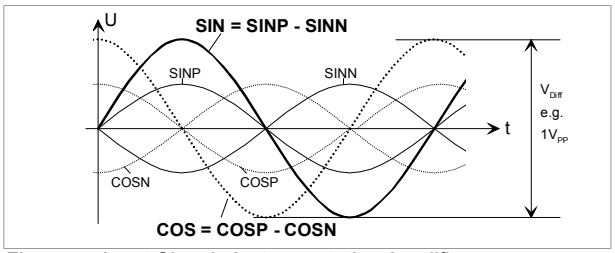


Figure 4 Input Signals Instrumentation Amplifier

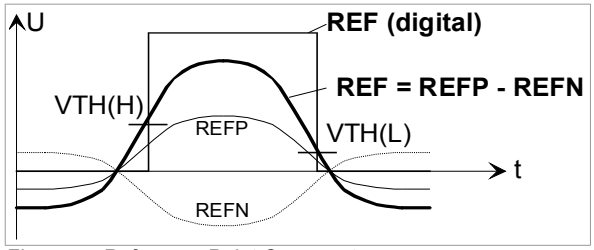


Figure 5 Reference Point Comparator

Table 6 Description Input Amplifier

Pin GAIN	GND	AVDD	V0	Open
Input voltage for differential input [1] (mV_{pp})	500	333	265	40
Input voltage U_{Diff} nominal (mV_{pp})	1000	666	530	80
Input voltage range for U_{Diff} (mV_{pp})	600-1200	400-800	320-640	60-100
Lower reference point comparator threshold (mV nominal)	12	8	6	1
Upper reference point comparator threshold (mV nominal)	30	20	15	3

[1] *at each of the inputs SINP, SINN, COSP, COSN*

ⓘ *In case of using the IC with a nominal input voltage of 80mVpp, an external offset adjustment for sine, cosine and reference is recommended.*

6.2 Interpolation

The periods of the analogue signals sine (SIN) and cosine (COS) will be interpolated and output as 90 degrees phase shift square waves at the pins A and B. If a counter is connected which is able to realise a 4-fold evaluation the input signal will be split in up to 40 increments. The width of the reference pulse Z at the output is selectable between ¼ and 1 period of the signals A and B. The reference/index signal will be generated if the analogue signals sine and cosine have a phase angle of 45 degrees. At the same time the difference voltage at the reference inputs REFP and REFN must be beyond the thresholds. If the IC was configured for an output pulse width of one increment, the outputs A and B have to be high additionally.

Table 7 Reference Point Signal

IRATE	Phase angle reference signal Z	
	Width = 1 Increment = ¼ period	Width = 4 Increments = 1 period
40-fold	45° ... 54°	36° ... 72°
32-fold	45° ... 56.25°	33.75° ... 78.75°
20-fold	36° ... 54°	18° ... 90°
16-fold	33.75 ... 56.25°	11.25° ... 101.25°
8-fold	22.5° ... 67.5°	-22.5° ... 157.5° resp. like REFP/REFN
4-fold	0 ... 90°	Like the signals REFP/REFN

ⓘ *The position of the reference signal Z at the output is shift if the digital hysteresis is active. For interpolation rates 40 and 20 this shift is 1/40 of the sine period = 9°, and for all other rates the shift is 1/32 of the sine period = 11.25°.*

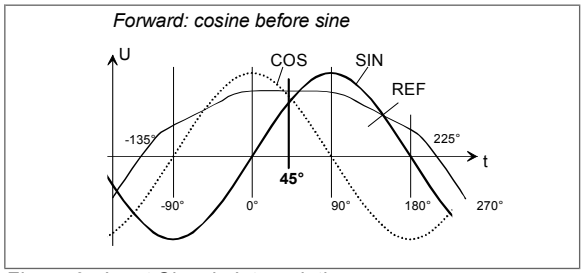


Figure 6 Input Signals Interpolation

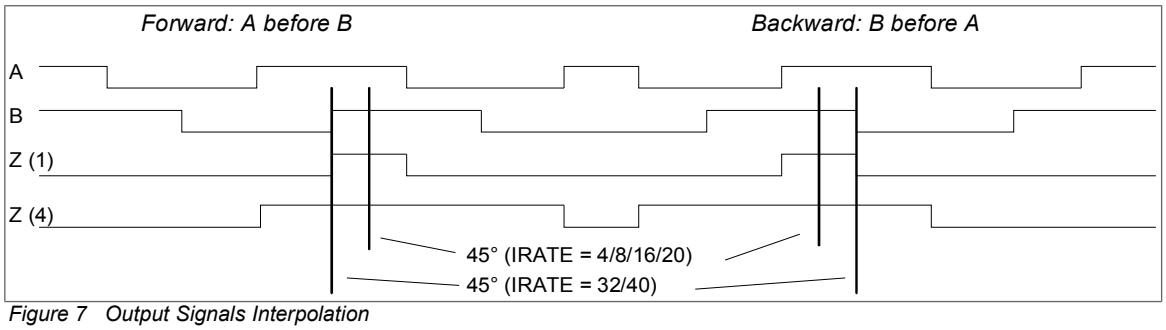


Figure 7 Output Signals Interpolation

6.3 Hysteresis

For eliminating the edge noise at lower input frequencies and at standstill an analogue and a digital hysteresis can be configured. The value of the analogue hysteresis is defined by the resistor at the pin RHYST. So a noise reduction for real time systems is possible without losing the synchronisation between input and output signals. If the digital hysteresis at the pin RHYST is active, the switching of the outputs in case of static input signals is eliminated. All output signals are delayed for one angle increment (9 degrees resp. 11.25 degrees)

The following figure shows the consequences of the digital hysteresis in case of a change of direction at the example of an interpolation rate 16 edges per period.

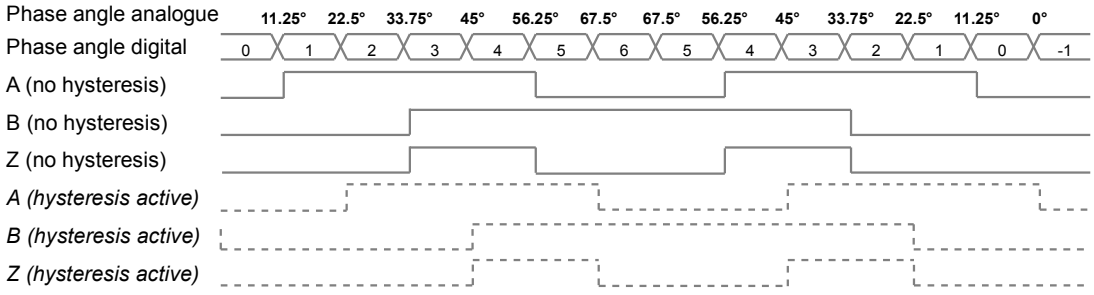


Figure 8 Digital Hysteresis

6.4 Edge Distance Control

The minimum distance t_{pp} at which the output signals A and B can switch is adjustable. After the switching of one of the outputs the following edge of the other signal occurs if the time t_{pp} was passed. So a following counter is able to count without error also in case of fast distortions. But there is no synchronisation with a clock. Usually the edges are generated without a delay.

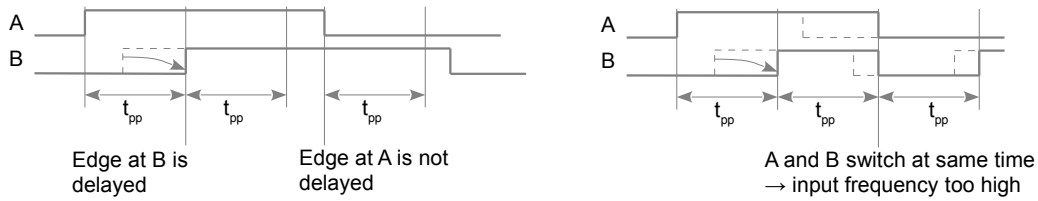


Figure 9 Minimum Edge Distance

The maximum input frequency is defined by the minimum A/B-edge distance and the interpolation rate. It is limited by errors of the input signals. An exceeding of this frequency is signalised by the same time switching of the outputs A and B. If the input frequency is higher than three times of the selected maximum frequency the behaviour of the outputs `A`, `B` and `Z` is not defined.

The configuration of the minimum edge distance can be done using the pin `RT`. A resistor to GND defines the time in the range of 30ns to 1ms. It has to be observed that this time can vary depending on exemplar and supply voltage. If the pin `RT` is connected to `AVDD`, the IC runs with the minimum A/B-edge distance of 33ns (Mode `TPP30`). This time can vary between 26ns and 40ns.

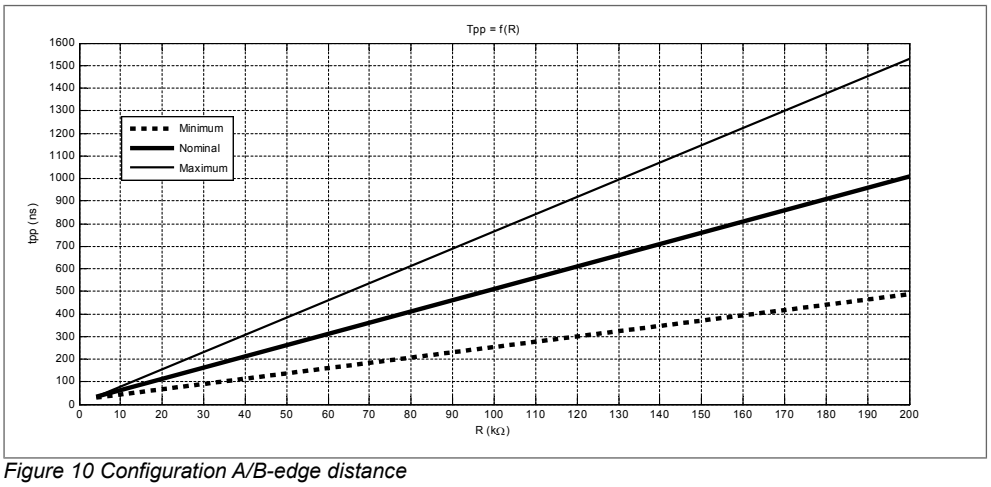


Figure 10 Configuration A/B-edge distance

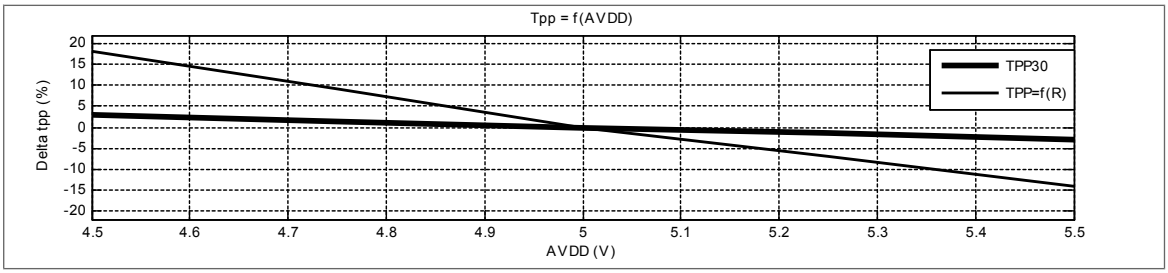


Figure 11 Dependence of the A/B-edge distance from the supply voltage

7 Parameters

Table 8 Absolute Maximum Ratings

Symbol	Parameter	Min.	Typical	Max.	Unit
VDD	Supply voltage			7.0 [3]	V
TJ	Operating temperature	-40		120	°C
TS	Storage temperature	-55		150	°C
V(AIN)	Voltage at the analogue inputs [1]	-0.3		AVDD+0.3	V
V(CFG)	Voltage at the configuration inputs [2]	-0.3		AVDD+0.3	V

[1] Pins SINP, SINN, COSP, COSN, REFP, REFN, [2] Pins RT, RHYST, GAIN, CFG0, CFG1, [3] t < 250ms, T < 60°C

Table 9 Operating Conditions

Symbol	Parameter	Min.	Typical	Max.	Unit
VDD	Supply voltage	4.5	5.0	5.5 [1]	V
I(AVDD)	Current consumption analogue		25	33	mA
I(DVDD)	Current consumption digital		3	5	mA
TOP	Operating temperature	-40 [1]		120	°C

[1] Minimal temperature and maximal voltage are not allowed at the same time; If TOP < -15°C then VDD must be ≤ 5.25V

Table 10 Parameters Analogue

Symbol	Parameter	Min.	Typical	Max.	Unit
Z(AIN)	Input impedance		1GΩ||8pF		
Gain	Gain (see table)	98	100	102	%
VMON	AC-Voltage at SMON and CMON nominal		2.4		V_{pp}
fg	Cut-off-frequency (attenuation 1dB) @ GAIN = GND/VCC/V0	1200			kHz
fg(80mV)	Cut-off-frequency (attenuation 1dB) @ GAIN = open (80mV_{pp})	250			kHz
Vos	Input offset voltage	-20		20	mV
φ(AIN)	Phase shift SIN/COS (f = 600kHz,GAIN = GND/VCC/V0)			30	°
VCM	Common mode input voltage range	0		3.7	V
CMRR	Common mode rejection ratio (@ f < 1kHz, GAIN = GND)	50			dB
U(V0)	Voltage at pin V0	2.10	2.25	2.40	V
VTH(REFL)	Lower threshold reference/index comparator		1.2		%VINNOM[1]
VTH(REFH)	Upper threshold reference/index comparator		3		%VINNOM[1]
I(V0)	Output current at pin V0			0.5	mA

[1]Nominal value of the differential voltage SINP-SINN resp.. COSP-COSN

Table 11 Parameters Interpolation

Symbol	Parameter	Min.	Typical	Max.	Unit
fIP_40	Input frequency @ IR = 40,GAIN = GND/VCC/V0	0		600	kHz
fIP_32	Input frequency @ IR = 32,GAIN = GND/VCC/V0	0		750	kHz
fIP	Input frequency @ IR = 20/16/8/4,GAIN = GND/VCC/V0	0		1200	kHz
fIP_80mV	Input frequency @ GAIN = open	0		250	kHz
EABS	Absolute angle error [1]		± 0.5	± 0.9	Increments
EDIFF	Differential angle error [1]		± 0.3	± 0.4	Increments
Tpp(L)	Minimum edge distance @ Pin RT = L	25		1700	ns
Tpp(H)	Minimum edge distance @ Pin RT = H	26	33	40	ns

[1] Input voltage range 1V_{pp}

Table 12 Parameters Configuration / Parameters Digital

Symbol	Parameter	Min.	Typical	Max.	Unit
VOH	Output voltage H [1)]	80			%DVDD
VOL	Output voltage L [1)]			0.4	V
I(DIG)	Output current digital [1)]			4	mA
VTH(L-O)	Threshold voltage L / open [2)]	7	10	13	%DVDD
VTH(O-V0)	Threshold voltage open / V0 [2)]	33	36	39	%DVDD
VTH(V0-H)	Threshold voltage V0 / H [2)]	87	90	93	%DVDD
V(CFGO)	Clamping voltage if open [2)]	1.10	1.15	1.20	V
VTH(RHyst)	Threshold voltage L/H, Pin RHYST		50		%DVDD
VTH(RT)	Threshold voltage L/H, Pin RT		85		%DVDD
R(RHYST)	Configuration resistor hysteresis	47	250	250	kΩ
R(RT)	Configuration resistor edge distance	4		200	kΩ

1) Pins A, B, Z
2) Pins CFG0,CFG1,GAIN

8 Application Notes

8.1 General Information

- All IC-inputs have to be connected to a defined level
- Blocking capacitors are required at pins AVDD and DVDD.
- A 100nF capacitor is required at pin V0.
- In case of open pins CFG1 or CFG0, the wiring length has to be shorter than ≤ 10cm at these pins, otherwise an additional 1nF capacitor has to be connected to the IC-pin directly.

8.2 4-State Logic

In order to bring together all possibilities for configuration with a small package size, the AIP40 contains 4-state logic pins. Normally these pins are controlled via soldering pads to minimize PCB-space. If the system includes a microcontroller, connection possibilities are available as follows:

Version 1 – Two CMOS controller pins, able to tristate

Connect Pin A to configuration pin directly, connect Pin B to configuration pin via a resistor of 68...75 KΩ.

Table 13 configuration pin connected to two controller pins

Pin A	Pin B	Voltage at configuration pin	State
L	Z	<0.4V	Low
H	Z	>4.7V	High
Z	Z	about 1.15V	open
Z	H	about 2.5V – 3.5V	V0

Version 2 – One controller pin; renunciation of configuration possibilities

By controlling each configuration pin directly by one controller pin, AIP40 configurations can be activated as follows:

Table 14 Overview interpolation rates - configuration pin directly connected to a controller pin

Interpolation rate	Output Z	Digital controlled	Digital and tristate controlled
40	1 Inkrement	√	√
32	1 Inkrement	√	√
20	1 Inkrement		
16	1 Inkrement		√
8	1 Inkrement		
4	1 Inkrement		
40	4 Inkrement	√	√
32	4 Inkrement	√	√
20	4 Inkrement		
16	4 Inkrement		√
8	4 Inkrement		√
4	4 Inkrement		√

Table 15 Overview Gain - configuration pin directly connected to a controller pin

Amplitude (nominal)	Digital controlled	Digital and tristate controlled
1 V_{pp}	√	√
666mV_{pp}	√	√
530mV_{pp}		
80mV_{pp}		√

8.3 Sensor Adjustment

To check and adjust the sensor, the output signals of the instrumentation amplifier are monitored at the pins SMON and CMON. For fine tuning of the sensor signals the output signals A, B and Z can be used. For this the IC has to run with interpolation rate IRATE= 4-fold resp. IRATE= 8-fold.

Table 16 Sensor Adjustment

No.	Setting	Mode	CFG1	CFG0	Instruction
1	Amplitude sine /cosine	any	any	any	Measurement at the pins SMON and CMON Adjust sensor until both amplitudes are approx. 2.4 V_{pp}
2	Offset cosine	IR: 4-fold Z: 4 inc.	Open	AVDD	Moving of the sensor; Measurement at pin A Adjust sensor until duty cycle at A is 50% of periode on CMON.
3	Offset sine	IR: 4-fold Z: 4 inc.	Open	AVDD	Moving of the sensor; Measurement at pin B Adjust sensor until duty cycle at B is 50% of periode on SMON.
4	Reference	IR: 4-fold Z: 4 inc.	Open	AVDD	Moving of the sensor; Measurement at pin Z Adjustment until signal width is approximately the period of the sine signal
6	Amplitude ratio sine/cosine	IR: 8-fold Z: 4 inc.	Open	GND	Moving of the sensor; Measurement at A or B Adjustment until all edges uniformly distributed within the sine periode (duty cycle A/B is 50%)

8.4 Application circuits

Sensor with differential outputs

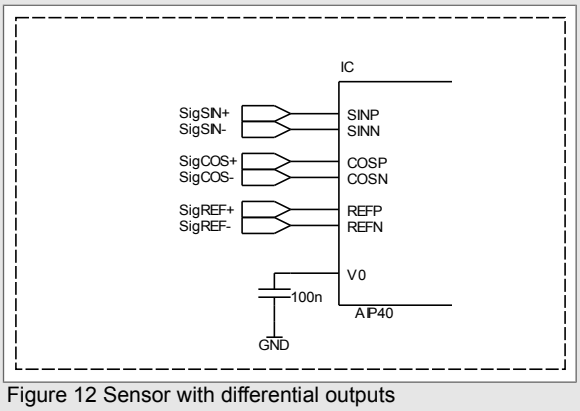


Figure 12 Sensor with differential outputs

- Setting of GAIN-pin is defined by the amplitude of the input signals.
- Reference level V0 is generated internal.

Sensor with Single-ended outputs

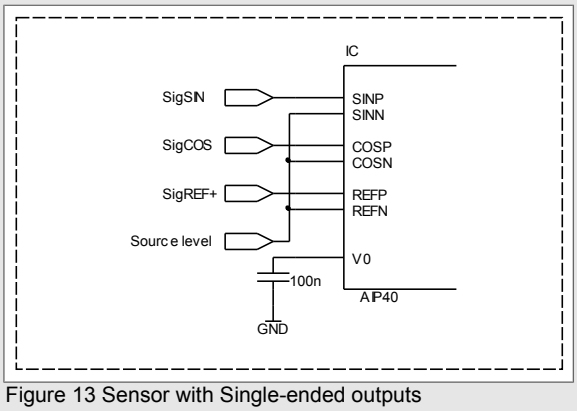


Figure 13 Sensor with Single-ended outputs

- Setting of GAIN-pin is defined by the amplitude of the input signals.
- Reference level V0 is generated by sensor (Source level).

Sensor with Single-ended outputs

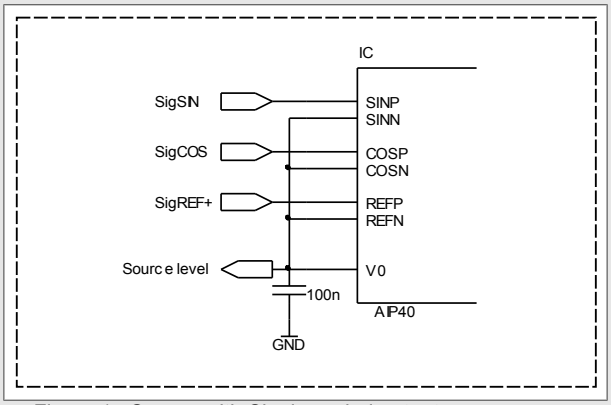


Figure 14 Sensor with Single-ended outputs

- Setting of GAIN-pin is defined by the amplitude of the input signals.
- Reference level V0 is generated by the AIP40 (Dest level).
- The maximal current at pin V0 is 500µA.

Sensor with current outputs or sensor containing photodiodes

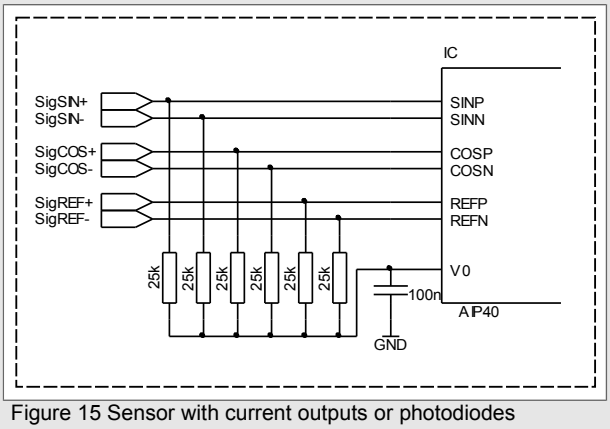


Figure 15 Sensor with current outputs or photodiodes

- GAIN-pin has to set an amplitude of 530mV nominal. (connect to V0)
- External resistors between input signals and V0-pin are required.
- Shown resistor value of R=25kW is suitable for an amplitiude of 11µApp. It has to be adjusted to the given sensor:
  R = 530mV / (2·Inom)

Sensor without reference signals

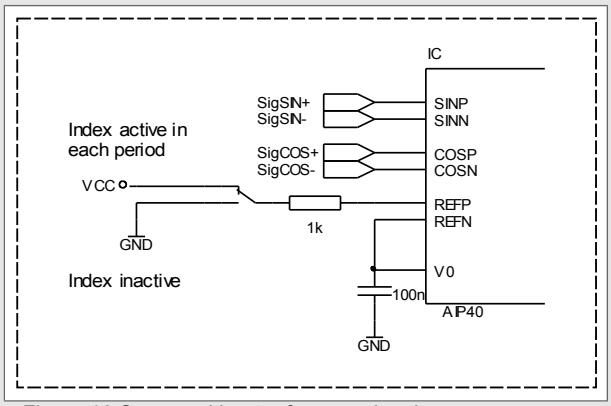


Figure 16 Sensor without reference signals

- A defined state at Z-output (active or inactive) will set via the pins REFP and REFN

Configuration

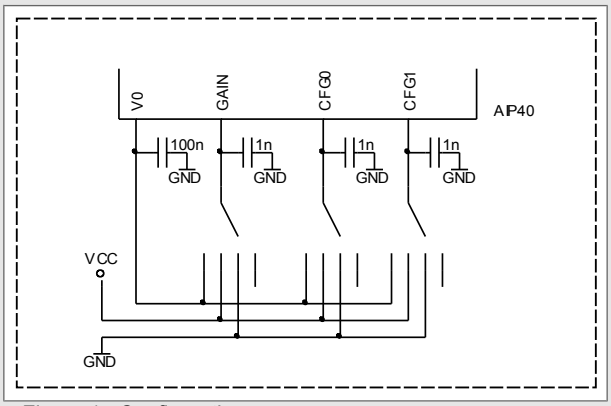


Figure 17 Configuration

- The pins GAIN, CFG0 und CFG1 are set by a 4-value logic. To choose a configuration each of this pins can left open or can be connected to 3 different levels (VCC, GND, V0).
- Please refer chapter “Configuration” for a detailed description.

Square wave outputs

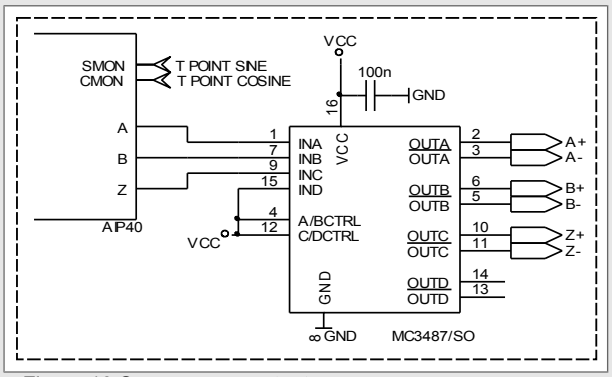


Figure 18 Square wave outputs

- The outputs A, B and Z are CMOS outputs which can drive max. 4 mA. To realize a RS422-interface an external line-driver is required.

A/B-edge distance and hysteresis

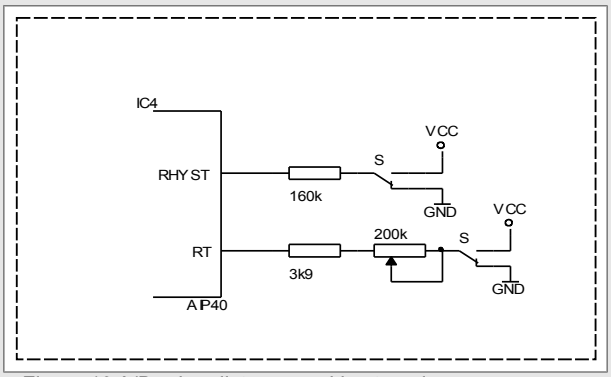


Figure 19 A/B-edge distance and hysteresis

- To configure the minimal A/B-edge distance and the a digital and analogue hysteresis the shown circuit is used for.
- Further information can be found in the chapters 6.3 and 6.4.

Sensor with anti-parallel photodiodes - Possibility of adjustment for amplitude equality

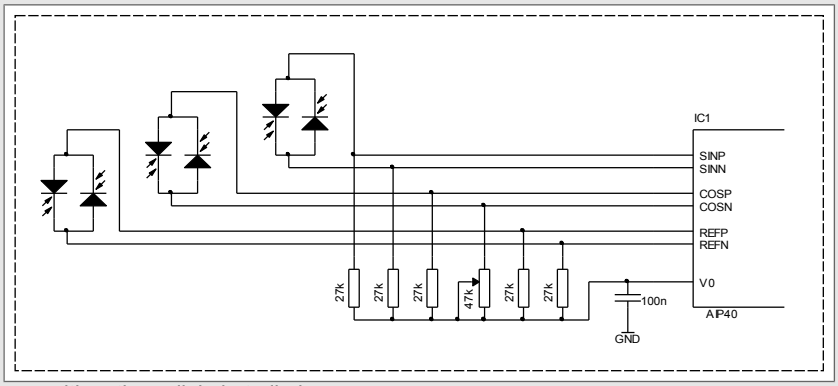


Figure 20 Sensor with anti-parallel photodiodes

- To avoid distortions the nominal amplitude of the AIP40 has to be set to 530mVpp or 80mVpp for this kind of sensors
- The amplitude equality is adjusted by changing the amplitude of the cosine signal. The pins SMON and CMON are used for the measurement.
- The shown resistor values are valid for sensors of 10µApp and an AIP40 nominal amplitude of 530mVpp.
- The resistor value is given by: R = Vnom / (2·Inom) and PAmpl ≈ 1.5·R

Sensor amplitude / Nominal amplitude AIP40	80mVpp	530mVpp
$11\mu A_{pp}$	R = 3.6k / P_{Ampl} = 5k	R = 24k / P_{Ampl} = 33k
$16\mu A_{pp}$	R = 2.5k / P_{Ampl} = 3.9k	R = 18k / P_{Ampl} = 27k

Photodiode array with common cathode / common anode - Possibilities of adjustment for amplitude equality and offset

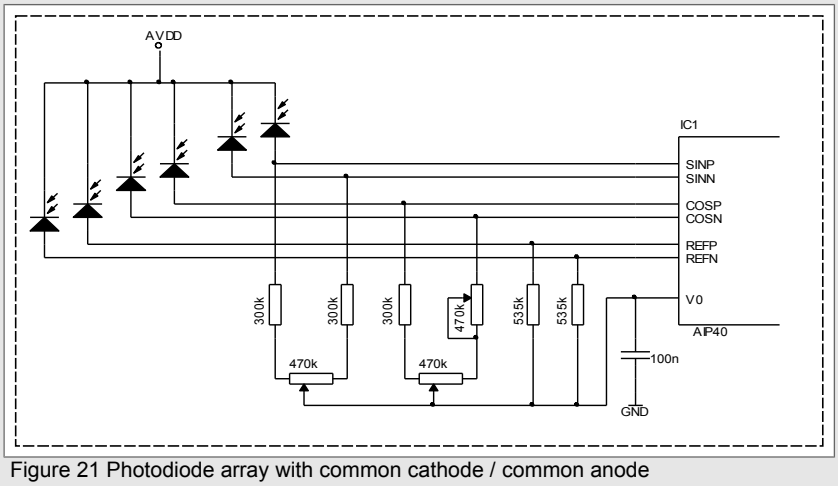


Figure 21 Photodiode array with common cathode / common anode

- First the amplitude equality has to be adjusted by changing the amplitude of the cosine signal. Then the offset for both signals can be adjusted. The pins SMON and CMON are used for the measurement.
- The shown resistor values are valid for sensors of 0.5µApp and an AIP40 nominal amplitude of 530mVpp.
- The resistor value is given by: R = Vnom / (2·Inom). This resistor is partly designed as a potentiometer for the adjustment of the offset: POffs ≈ R; RFIX = R-½POffs; PAmpl ≈ 1.5·RFIX

Sensor amplitude / Nominal amplitude AIP40	80mVpp	530mVpp
$0.5\mu A_{pp}$	R_{FIX} = 30k / P_{Offs} = 100k / P_{Ampl} = 47k	**R_{FIX} = 300k / P_{Offs} = 470k / P_{Ampl} = 470k**
$11\mu A_{pp}$	R_{FIX} = 1.2k / P_{Offs} = 5k / P_{Ampl} = 2k	R_{FIX} = 13k / P_{Offs} = 22k / P_{Ampl} = 22k

Sensors with a nominal amplitude of 2Vpp

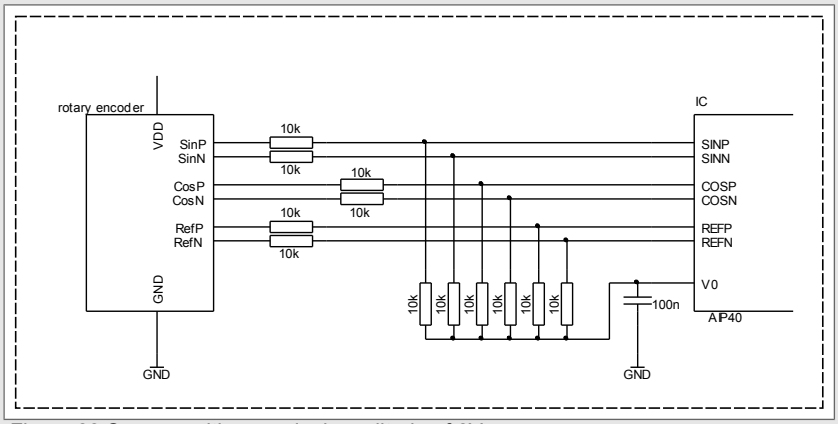


Figure 22 Sensors with a nominal amplitude of 2Vpp

- The input amplitude of the AIP40 is set to 1Vpp nominal at pin GAIN
- External resistors between the input signals and pin V0 are used as voltage divider for the sensor signals. The amplitude of the sensor signals will be divided by 2.

Standard application

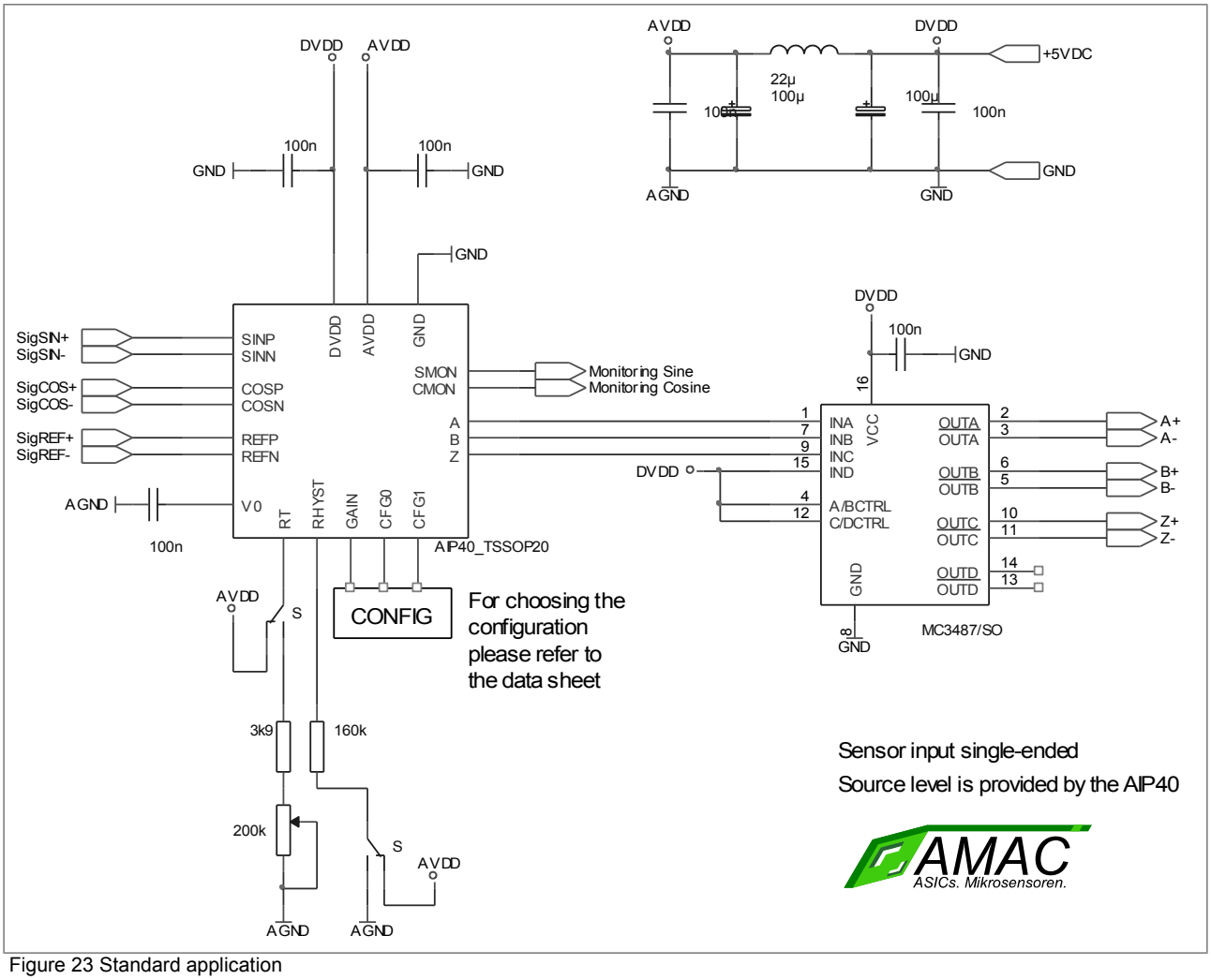


Figure 23 Standard application

9 Notes