IPE16000-USB

User Manual

Version: 1.2
Date: 09/03/2017

AMAC ASIC- und Mikrosensoranwendung Chemnitz GmbH
Kopernikusstr. 16
D-09117 Chemnitz
Germany

Tel.: +49 371 334204 - 0
Fax: +49 371 334204 - 69
E-Mail: info@amac-chemnitz.de
Web: www.amac-chemnitz.de

Revision Overview

Date	Revision	Change(s)
01.02.2013	1.0	First version
06.12.2013	1.1	Modification Overview features
09/03/2017	1.2	change to new AMAC document layout

Table of Content

List of Tables

List of Figures

Terms, Definitions and Abbreviations

AIP	–	Analog Interpolator Module
AVSS	–	ground analog (GND)
AN	–	square-wave signal A negative
AP	–	square-wave signal A positive
BN	–	square-wave signal B negative
BP	–	square-wave signal B positive
COS	–	cosine signal (P = positive; N = negative)
DVDD	–	supply voltage digital (+ 5 V)
DVSS	–	ground digital (GND)
EN	–	error signal negative
EP	–	error signal positive
REF	–	reference signal (P = positive; N = negative)
RS422	–	EIA-422 (conduction-bound differential serial data transmission)
SENSVDD	–	supply voltage analog (+ 5 V)
Sin	–	sinusoidal signal (P = positive; N = negative)
SPI	–	serial peripheral interface
V0	–	mean voltage
Vpp	–	peak-to-peak voltage
ZN	–	square-wave signal Z negative
ZP	–	square-wave signal Z positive

1 Overview

The interpolation unit IPE16000 – USB was designed to increase the resolution for incremental position and angular measuring systems with sinusoidal output signals offset by 90°. The IC inside divides the signal period up to 16384 times. Incremental encoders with voltage interface can be connected directly. The interpolation unit may operate with both differential and single – ended input signals. The configuration of the board is possible either via EEPROM, or via USB.

The internal AIP-Module performs a permanent correction of the input signals during operating time and allow a multiplication of the signals to the factor32. The input signals are subjected to an AMAC-specific internal gain and offset control. The phase displacement of the input signals can be corrected as well. The quality of the signals issued by the sensors is monitored in the internal interpolation circuit GC – IP2000.

The unit can be connected via the RS422 to a standard counter or controls. The internal power supply voltage is 5 VDC.

In addition, several build in functions of the interpolation circuit GC – IP2000 like switchable analog filter or a digital hysteresis make the unit an ideal choice for use in control systems.

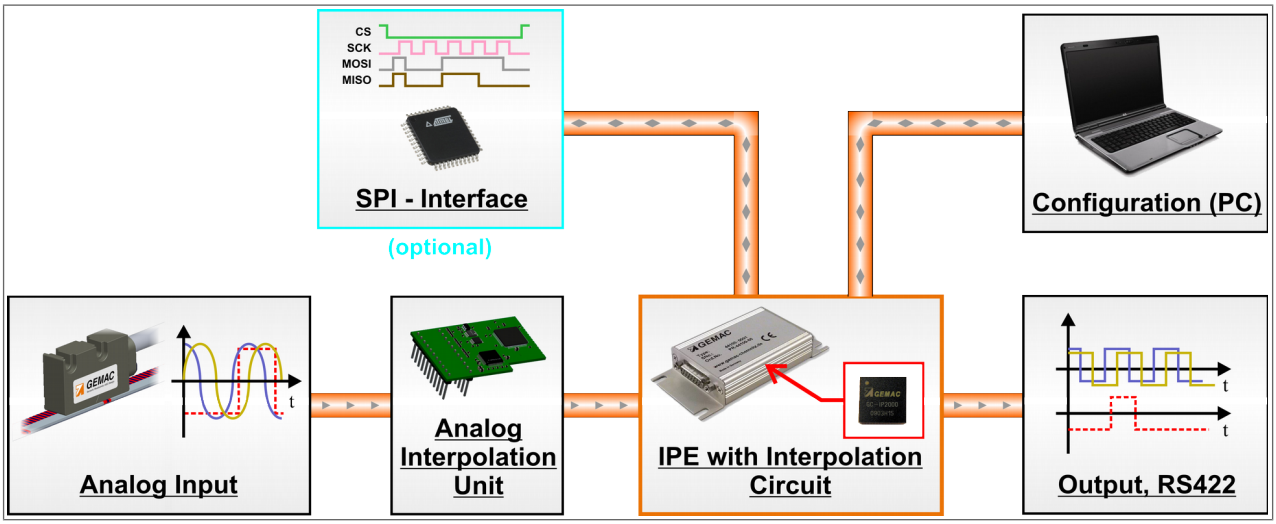

Figure 1: Block diagram

The IPE16000-USB has a processing in two steps. In first step the analog signals are corrected (0.1 Vpp … 4 Vpp) and multiplied (up to 32 times). In the second step the signals are transmitted to the GC-IP2000-circuit. The GC-IP2000 divides the signal period up to 2048 times.

Note:
Detail description of all functions can be found in the data sheet of GC – IP2000.

2 Features

Table 1: Overview features

Analog Part	
Analog Input	- Sine / cosine / reference (index) signals; differential or single ended - Input frequency max. 15 kHz - atomatically adjusted gain (0,1 V_{pp} – 4 V_{pp})
Digital Part	
Interpolation Rate	(100 / 128 / 200 / 256 / 400 / 500 / 512 / 800 / 1000 / 1024 / 1600 / 2000 / 2048)*(1...8)
Output Signals	- 30-bit counter value via USB, serial interface (SPI) optional - Frequency of edge change (A/B/Z) → maximum 24 MHz - 90° square-wave sequences (A/B/Z) - Error signal - Auxiliary signals for sensor adjustment - RS422 interface - 5V
Signal Correction	- free definable supporting point correction (up to 1024 supporting points) - AMAC-specific digital controller for the offset, control range ±10 % of standard amplitude - AMAC-specific digital controller for the amplitude and offset - Digital potentiometer with 40 steps for phase correction; selectable range ±5° or ±10° - LED control signal
Possibilities of configuration	Either: via USB, EEPROM or, if the option is ordered, via serial interface (SPI)
Optional SPI (internal interface)	- Compatible to the standard SPI: 16-bit, MSB first - SPI clock up to 25 MHz - For configuration and measuring value output; not required for trivial systems - 5V interface
Miscellaneous	
Suppression of disturbances	- Selectable analog noise filter - Digital hysteresis for suppression of the edge noise at the output
Adaptation of IC to subsequent devices	- Adjustable minimum edge interval at the output - Behaviour of IC in case of sensor error can be programmed - Adjustable width zero signal Z of ¼ or 1 period A/B

3 Ordering Information

Table 2: Ordering Information

Product Type	Description	Article Number
IPE16000 – USB	Interpolation Unit with AIP-Module and IP2000 (standard configuration)	PR-44120-00

4 Input Signals

The input signals of the IPE16000 – USB are analog voltages (sine / cosine), which have a sine – shaped dependency on the measured value (position or angle). The phase shift between those two analog voltages is 90°, related to one period of the scale. A third input signal serves the zero or reference point of the scale as reference signal for determining. All the tree input signals are processed as differential or single – ended signals.

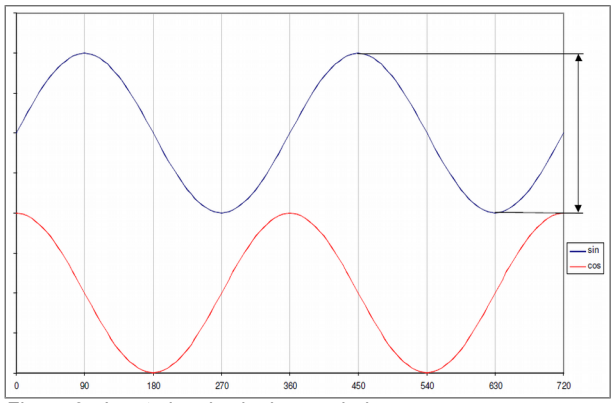

Figure 2: Input signals single – ended

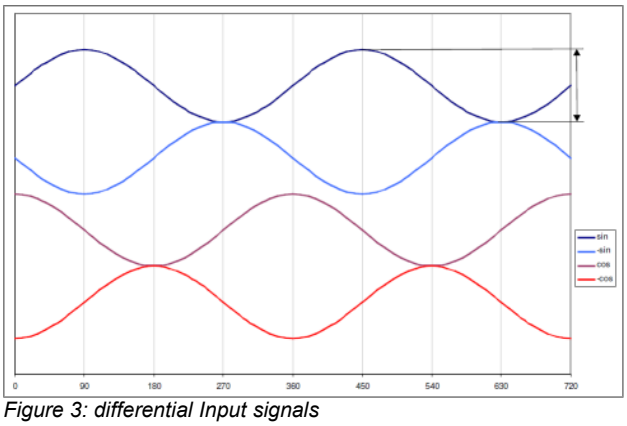

Figure 3: differential Input signals

4.1 Input Signals

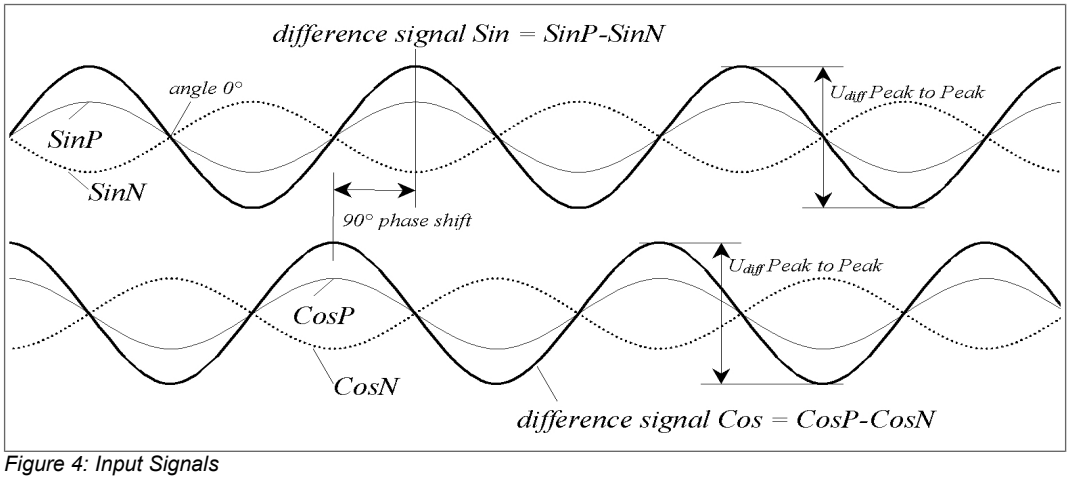

Figure 4: Input Signals

4.2 Input amplifier

The IPE16000-USB has a fully differential input stage which performs a correction of the input signals over a large voltage range (0,1 V_{pp} to 4 V_{pp}) during operating time. In addition, a multiplication of the input signal can be configured with a factor from 1 to 32. The synthetic Sine / Cosine signals which were generated on the input stage are fed to the interpolation circuit GC-IP2000. The conditioned and multiplied analog Signals in combination with the interpolation circuit GC-IP2000, reach an interpolation rate up to 16384.

4.3 Signal correction

The input signals are subjected to an AMAC-specific internal gain and offset control. The amplitudes are controlled in the range between 0.1 V_{pp} and 4 V_{pp} of the standard amplitude. The control range for the offset of the two signals is ± 10 % of the nominal amplitude. The phase shift of the input signals can be adjusted statically by the internal potentiometer in a range of ± 5° or ± 10°.

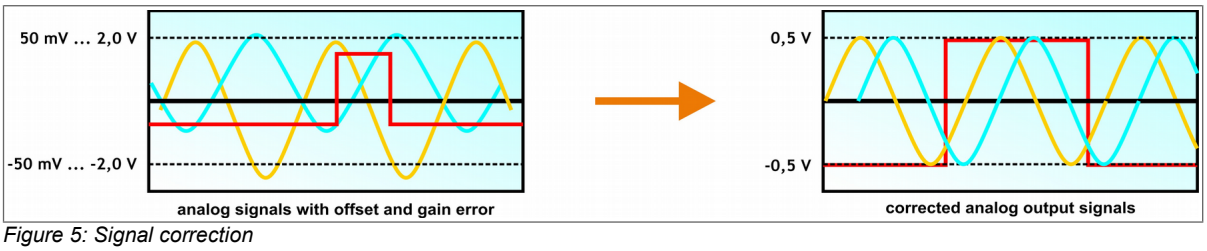

Figure 5: Signal correction

4.4 Reference Signal

The reference signal of measuring systems is typically called reference, index point or zero point signal. The reference signal is detected, if the voltage on input pin REFP is bigger than voltage on input pin REFN.

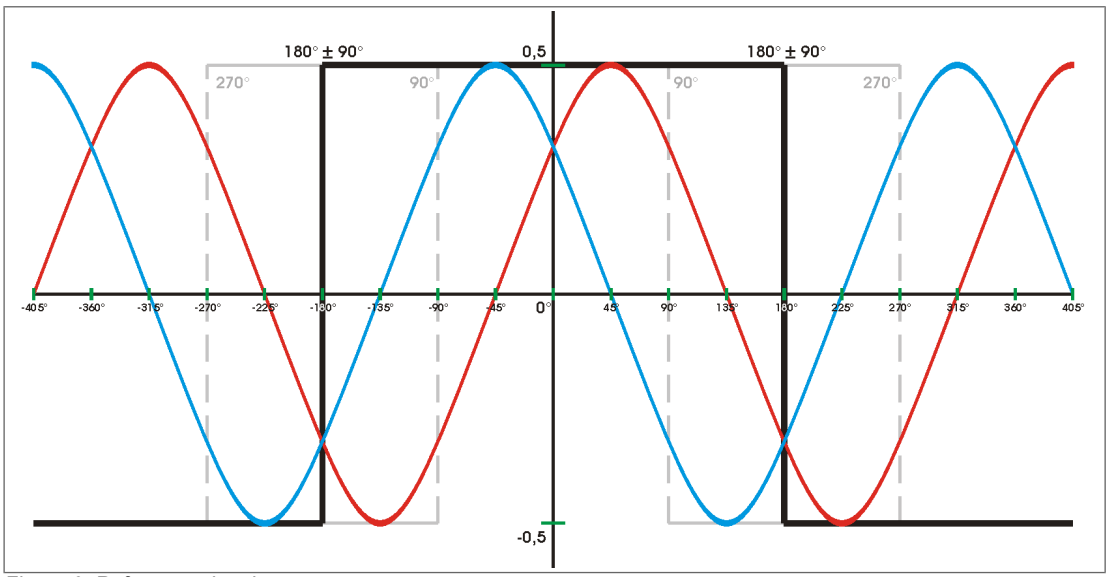

Figure 6: Reference signal

Note:
The reference point processing in the IPE16000 – USB can be deactivated in the internal configuration if no detection of the reference signal is needed.

Table 3: Reference signal intern

Register value CFG1 / DISZ	Meaning
0	Reference signal at the output active
1	Reference signal at the output inactive

Note:
The shape of the Z – signal on the output of the IPE16000 – USB can be adapted for different applications in the configuration of the interpolation circuit. Is one increment selected for the width of the Z – signal, the Z – Impuls on the output corresponds exactly one quarter of the period duration of the signals A and B. The Z – Impuls extends over a whole period when four increments are selected.

Table 4: Configuration of the reference point

Register value CFG1 / Z4	Meaning
0	1 increment = ¼ period
1	4 increments = 1 period

5 Output Signals

5.1 RS422

The output signals are phase shifted square wave sequences (known by incremental measuring transducers). They can be counted in a single or quadruple way. A synchronous Z – Impuls will be generated when the angle of 45° (refer also to Figure 4) is passed through and when the analogue differential input voltage between **REFP** and **REFN** exceeds the positive comparator hysteresis level. If the differential input voltage is permanently above this level, the reference pulse will be generated once during every signal period. The output signals are differential AP – AN, BP – BN, ZP – ZN.

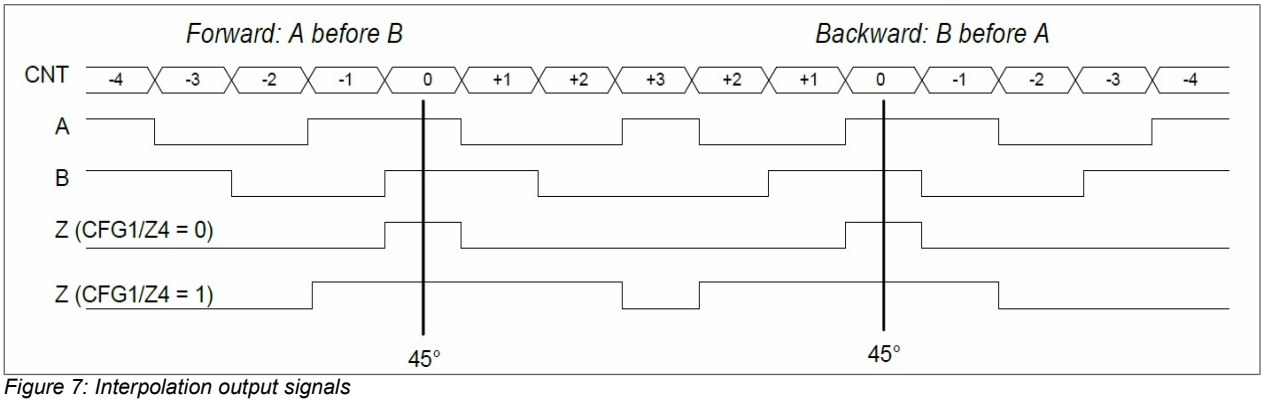

Figure 7: Interpolation output signals

Note:
The Signals A, B and Z are offset in time by 1 increment if the digital hysteresis is activated.

5.2 Error Signals

An error signal will be generated if the input signals are plausible no longer. The error signal will also be generated if the input frequency is so high that the square-wave signals are unable to follow, and/or when the maximum input frequency is exceeded. It is recommended to use the error signal for data processing.

Note:
If the error signal was detected, the current measuring results and the following results should be discarded. Following elimination of the cause of the error and a reset of the error bit, the reference point has to be passed by for absolute value measurements once again!

6 Interpolation Rate

6.1 Analog Interpolation

As a result of the signal noise ratio a maximum multiplication up to factor 8 is useful. The interpolation rate of the IPE16000-USB is a result from multiplication of the interpolation rate of the IP2000 and of the multiplication factor of the input stage.

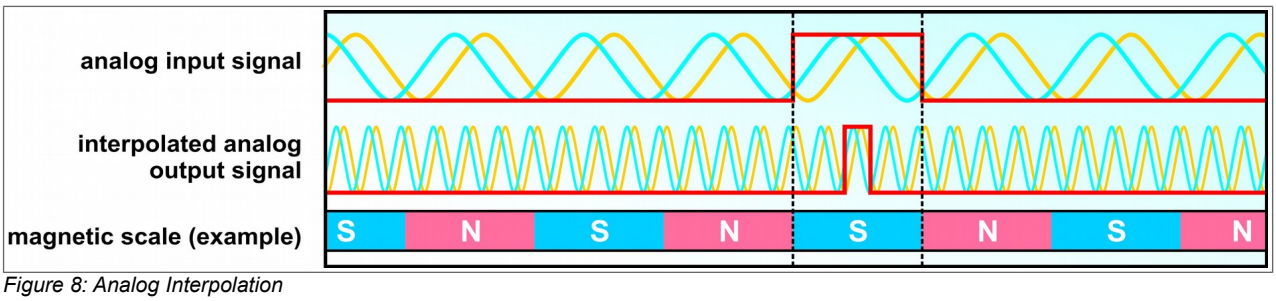

Figure 8: Analog Interpolation

6.2 Interpolation rate GC-IP2000

Possible interpolation rates (IRATE) which can be selected are 2048, 2000, 1600, 1024, 1000, 800, 512, 500, 400, 256, 200, 128 or 100. The term 'interpolation rate' is here understood as the number of increments into which the sinusoidal / cosinusoidal period of the input signals is divided.

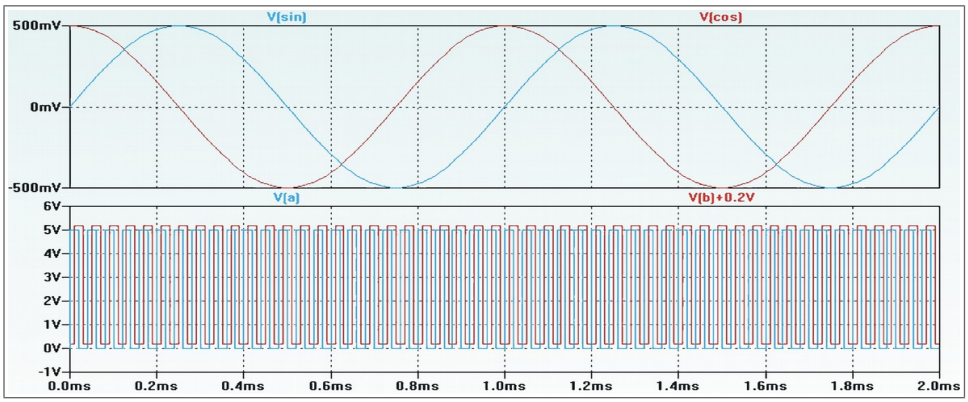

Figure 9: Interpolation rate GC-IP2000

Table 5: Configuration of the interpolation rate

Interpolation rate	CFG1 – IR(3:0)
2000	0000 (0)
1600	0001 (1)
1000	0010 (2)
800	0011 (3)
500	0100 (4)
400	0101 (5)
200	0110 (6)
100	0111 (7)
2048	1000 (8)
1024	1001 (9)
512	1010 (10)
256	1011 (11)
128	1100 (12)
1000	1101 (13)
1000	1110 (14)
1000	1111 (15)

6.3 Edge interval setting

The minimum time interval t_{pp} at which the output signals A,B and Z may switch can be adjusted in binary steps between 1/f_{OSZ} and 128/f_{OSZ}. This function can be used to restrict the bandwidth of the IPE2000 – USB for slow RS422 – Counters.

Table 6: Minimum edge interval

Min. edge interval tpp	Register CFG1 – TPP(2:0)	Pin CFGTPP
1/fosz	000 (0)	VSS
2/fosz	001 (1)	VDD
4/fosz	010 (2)	V0
8/fosz	011 (3)	open
16/fosz	100 (4)	
32/fosz	101 (5)	
64/fosz	110 (6)	
128/fosz	111 (7)	

6.4 Glitch filter

To suppress the edge noise of the output signals at low input frequencies and standstill, a digital hysteresis can be activated for the signals A, B and Z. This prevents switching of the outputs with static input signals. In this case, all output signals are delayed by one increment.

Table 7: Configuration of the hysteresis

Pin CFGFILT	CFG1 – DHE	CFG1 – Bit 11	Digital hysteresis
VSS	0	1	Don't use this configuration
VDD	1	1	Don't use this configuration
V0	0	0	deactivated
open	1	0	activated

7 Specifications

Table 8: Specifications

Recommended Operating Conditions	Min.	Nom.	Max.	Unit
Supply voltages	4.75 (4.5) [1)]	5.0	5.5	V
Supply current		240		mA
Internal interface voltage		3.3 / 5.0		V
Mid – voltage V_{0BUF}	2.1	2.25	2.4	V
Output Current on V_{0BUF}			30	mA
Operating case temperature	- 20		80	°C

Analog Input Specifications	Min.	Nom.	Max.	Unit
Input frequency			15	kHz
Phase offset between SIN and COS		90		°
Peak to Peak input voltage SINN ⇔ SINP / COSN ⇔ COSP	0.1	1.0	4	V_{pp}
Phase deviation	4.5 / 9	5 / 10	9 / 11	°
Oscillator frequency		25		MHz

Interpolation	Min.	Nom.	Max.	Unit
Interpolation Rates	(100 / 128 / 200 / 256 / 400 / 500 / 512 / 800 / 1000 / 1024 / 1600 / 2000 / 2048)*(1...8)			
Minimum interval time A / B – Signals	1 / fosz		128 / fosz	ns
Interpolation accuracy		± 0.7		
Propagation delay square – wave outputs (A / B / Z)	155 / fosz		187 / fosz	ns

Other characteristics	Extruded aluminium housing
Degree of protection	IP20
Connector	SUB – D, 15-pin
Dimensions	55 mm x 80 mm x 20 mm

1) The control ranges and the interpolation accuracy are limited between 4.5 V and 4.75 V.

8 Configuration of the Connectors

8.1 Signal input X1, female

Table 9: Signal input SUB – D 15-pin; female

Pin	Name	Direction	Meaning
1	SINP	Input	Encoder signal sine positive
2	AVSS	Output	Encoder ground
3	COSP	Input	Encoder signal cosine positive
4	SENSVDD	Output	Encoder power supply 5V
5	–	–	–
6	–	–	–
7	REFN	Input	Encoder signal reference negative
8	–	–	–
9	SINN	Input	Encoder signal sine negative
10	AVSS	Output	Encoder ground
11	COSN	Input	Encoder signal cosine negative
12	SENSVDD	Output	Encoder power supply 5V
13	–	–	–
14	REFP	Input	Encoder signal reference positive
15	–	–	–

8.2 Signal output X2, male

Table 10: Signal output SUB – D 15-pin; male

Pin	Name	Direction	Meaning
1	AP	Output	Square wave Output A positive
2	DVSS	Input	Unit power supply ground
3	BP	Output	Square wave Output B positive
4	DVDD	Input	Unit power supply 5V
5	EN	Output	Error Output E negative
6	–	–	–
7	ZN	Output	Square wave Output Z negative
8	nTRGIN	Input with pullup	Trigger signal input; falling edge active
9	AN	Output	Square wave Output A negative
10	DVSS	Input	Unit power supply ground
11	BN	Output	Square wave Output B negative
12	DVDD	Input	Unit power supply 5V
13	–	–	–
14	ZP	Output	Square wave Output Z positive
15	EP	Output	Error Output E positive

8.3 Signal output X2, male with ordered SPI – option

Table 11: Signal output X2 with SPI

Pin	Name	Direction	Meaning
1	MISO	Output	SPI MISO
2	DVSS	Input	Unit power supply ground
3	SEN	Output	SPI SEN
4	DVDD	Input	Unit power supply 5V
5	EN	Output	Error Output E negative **not used**
6	–	–	–
7	ZN	Output	Square wave Output Z negative **not used**
8	nTRGIN	Input with pullup	Trigger signal input; falling edge active
9	MOSI	Input	SPI MOSI
10	DVSS	Input	Unit power supply ground
11	BN	Output	SPI SCK
12	DVDD	Input	Unit power supply 5V
13	–	–	–
14	ZP	Output	Square wave Output Z positive **not used**
15	EP	Output	Error Output E positive **not used**

8.4 USB interface X3

Table 12: USB interface X3

Pin	Name	Meaning
1	+ USB	+ 5 V
2	USBD -	Data -
3	USBD +	Data +
4	ID	–
5	- USB	GND

8.5 Analog output header X4, analog test signal sine / cosine

Table 13: Analog output header X4, analog test signal sine / cosine

Pin	Name	Direction	Meaning
1	SMON	Output	analog test signal sine
2	CMON	Output	analog test signal cosine
3	GND	Input	analog ground for measuring

8.6 LED

Table 14: LED

LED	Value	Meaning
Sensor monitor LD1 LD2		
	red (LD2 off)	Sensor adjustment necessary / Sensor not connected
	green (LD1 off)	Sensor signals valid
Power LED LD3		
	Off	IPE2000-USB not working
	green	IPE2000-USB working

9 Configuration of the GC-IP2000

9.1 Configuration Process

After the reset of the IC GC – IP2000, all registers are initialised with their default values. If an IPE16000 – USB unit with SPI – option is used, it should be noted that during the whole RESET sequence the Pin MISO / nWAIT is maintained at Low level. Subsequently, the configuration register can be modified via USB or if the SPI – option was ordered via the serial interface SPI. Therefore you have to use the program “IPE16k-Monitor” with the IPE16000 – USB unit. After installation according to the manual of the program the IPE16000 – USB must be connected to the PC. (refer also to Figure 10)

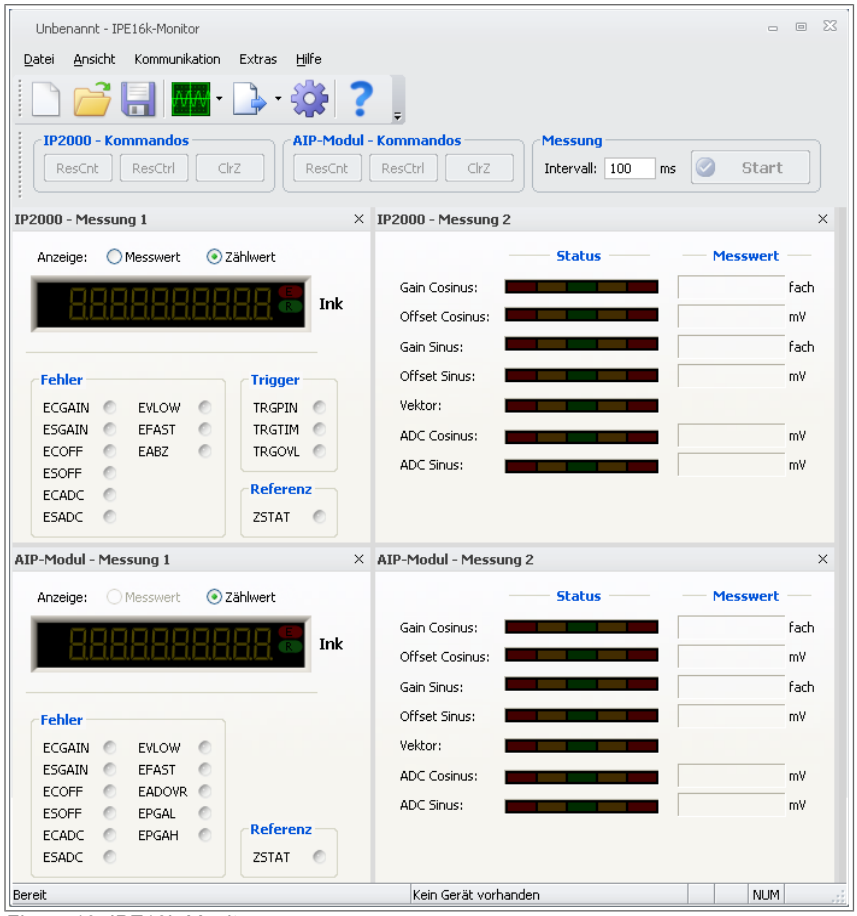

Figure 10: IPE16k-Monitor

9.2 Configuration with Softeare IPE16k-Monitor

The following functions differ from the description in the program manual:

- The checkbox for LEDMODE should always be empty because the LED Control Mode is not supported from the IPE16000 – USB.

10 Component Mounting Diagram

10.1 Component and solder side AIP-Module

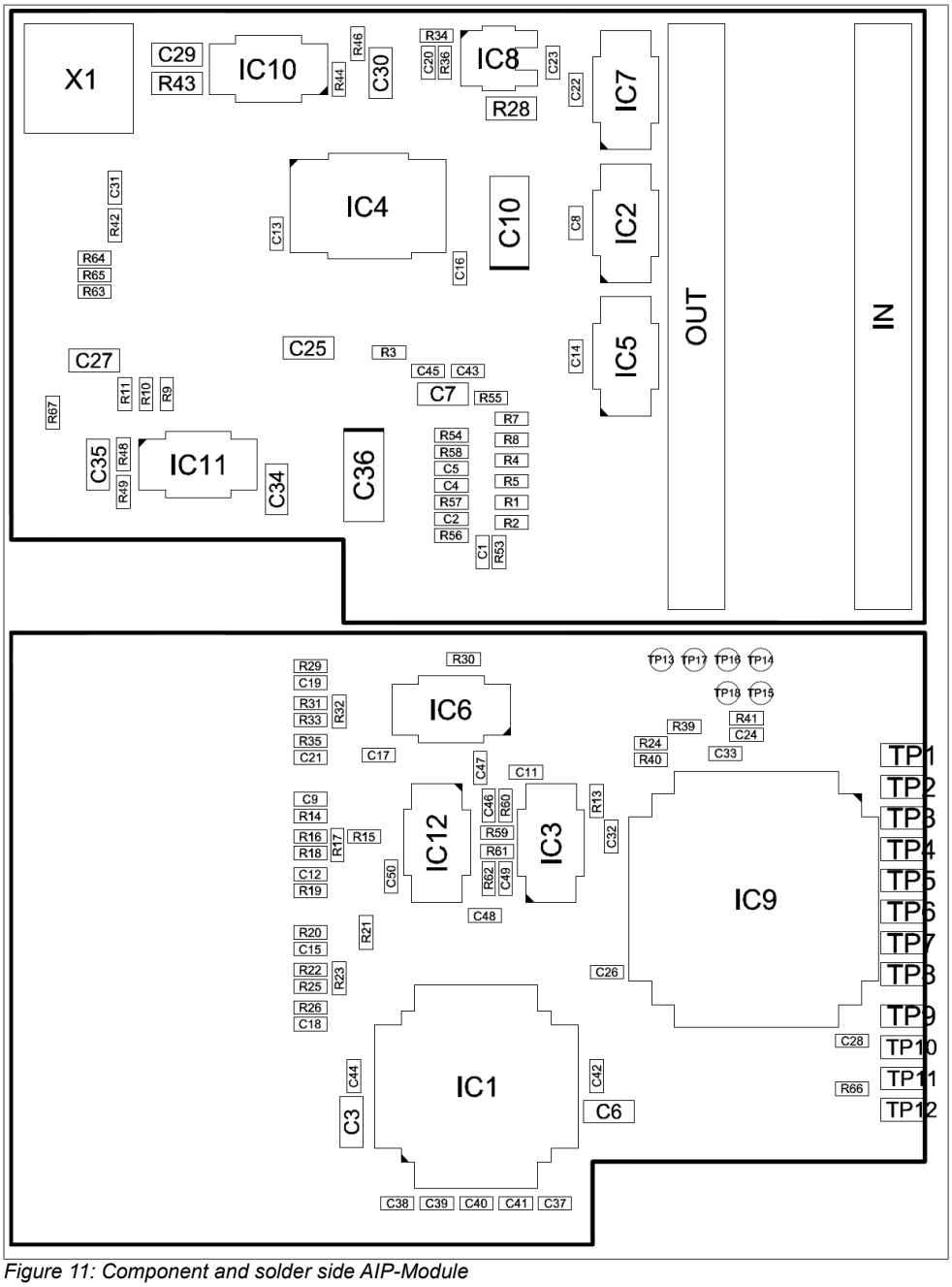

Figure 11: Component and solder side AIP-Module

10.2 Component side IPE-circuit board

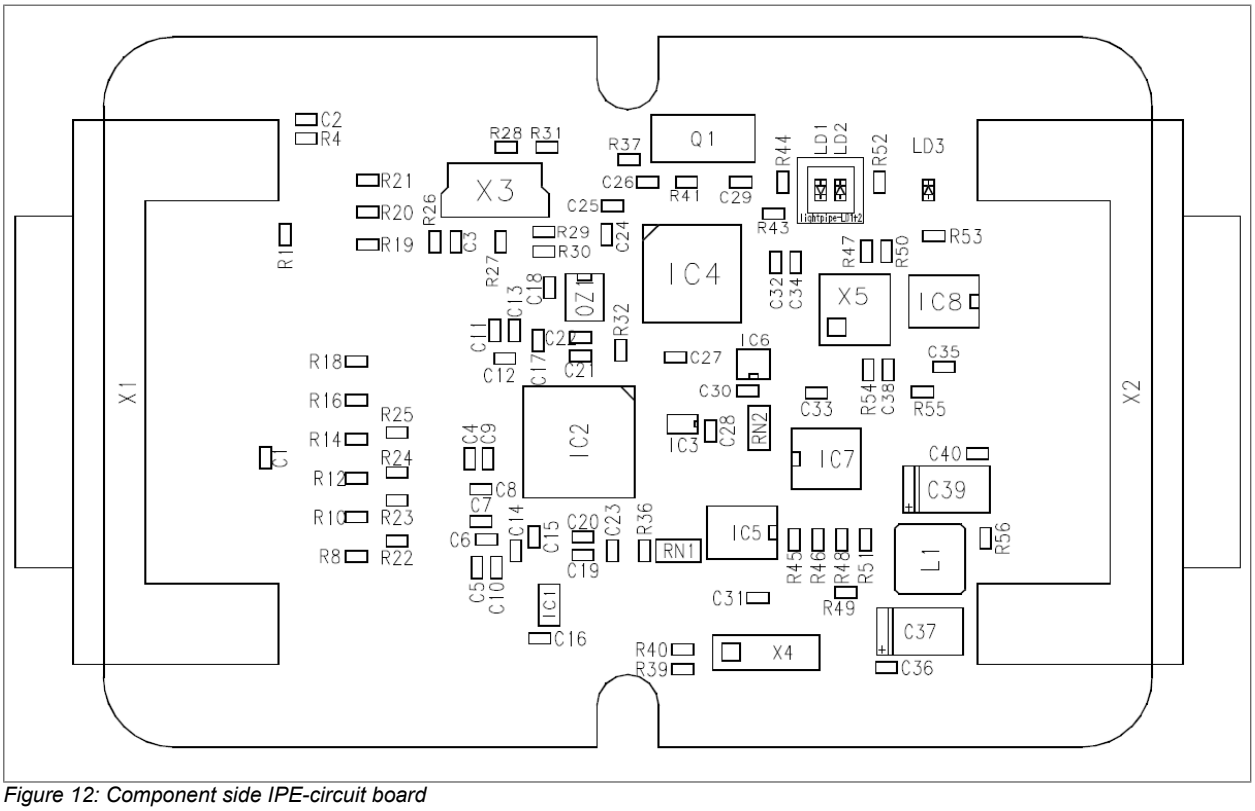

Figure 12: Component side IPE-circuit board

10.3 Dimensions

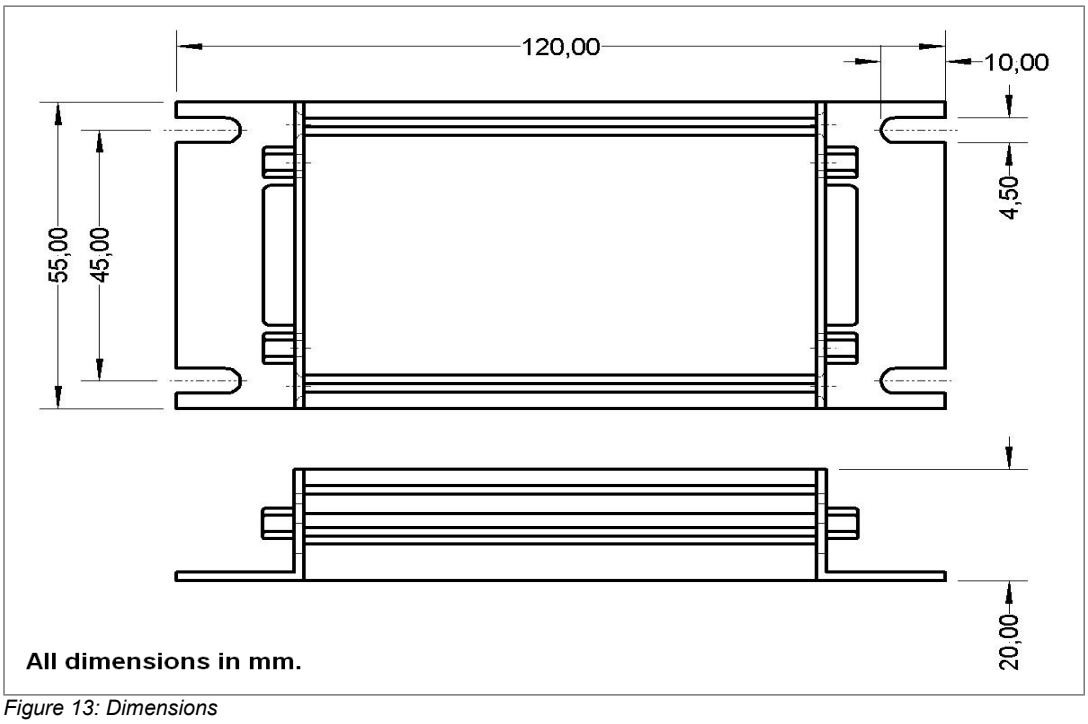

Figure 13: Dimensions

11 Notes