AM-IPE-NONIUS

User Manual

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1 Overview

The 2-channel interpolation unit AM-IPE-NONIUS serves to increase the resolution of absolute position and angular measuring systems with 2 sinusoidal output signals (nonius signal). Aside from the calculation of the absolute position, the AM-IPE-NONIUS may also operate as one- or two-channel incremental measuring system.
The AMAC nonius interpolation circuit GC-NIP inside the unit divides the periods of the input signals up to 8,192 times for calculating the incremental position on both channels as well as the absolute position using the nonius calculation with a resolution of up to 22 bit. To increase precision of the absolute position a set of sensor- or scale-specific correction coefficients can be placed in the EEPROM of the GC-NIP. Furthermore the input signals are subjected to an AMAC-specific internal gain and offset control. Additionally, the phase deviation of the input signals can be adjusted statically by a digital potentiometer. The noise of the sensor signals is prevented by a switching analogue filter. Additionally, a digital hysteresis can suppress the edge noise of the output signals at low input frequencies and at standstill. Thus, is case of short-time disturbance of the input signals, a subsequent interpolation counter will operate without errors.
The distance information can be passed on to processing components via a fast SPI interface, an SSI interface, a BiSS interface or by conventional ABZ-square-wave signals.

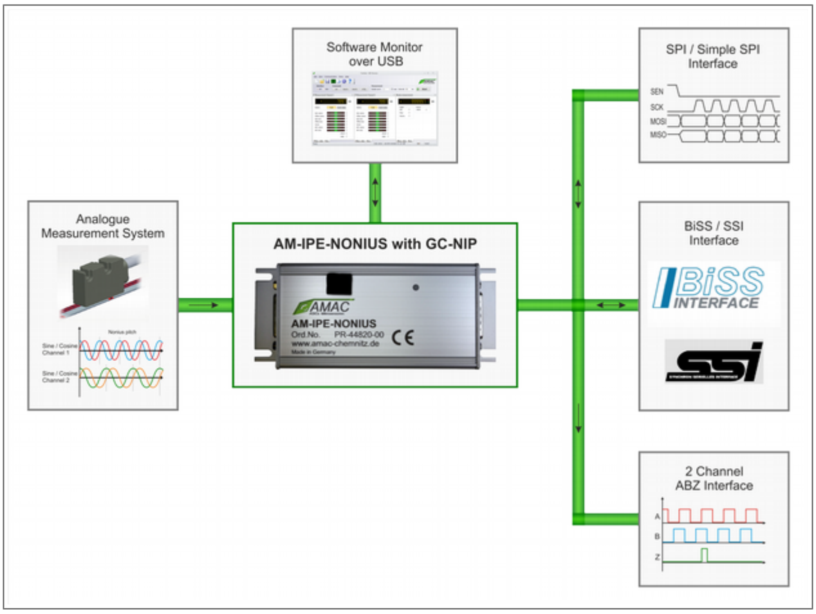


Figure 1: Block diagram

The quality of the signals issued by the sensors is monitored in the GC-NIP inside the AM-IPE-NONIUS. For that purpose it is possible to activate 9 sources separately producing an error signal. In that way, harmonics of the sinusoidal signals or inaccuracies of the measuring scale do not lead to errors in the absolute position value. The determination of the correction coefficients is realized by a simple software-based calibration procedure.
Encoders with voltage interface or measuring bridges can be connected directly. Sensors with current interface and photodiode-arrays are adapted by a simple external circuit. The Unit operates on both single-ended or differential input signals.
Providing absolute position and incremental square-wave-signals (ABZ) in parallel, the AM-IPE-NONIUS is well-suited for the use in motor-feedback-systems. The four integrated output interfaces (ABZ/SPI/SSI/BiSS) and further features like the multistage trigger signal processing, the processing of distance coded reference marks, the possibility to adjust the reference mark as well as adjustment and storage of the zero position make the IC suitable for direct use in industrial controls or in fast absolute or multichannel incremental position measuring systems. A selectable master SPI interface allows the user to modify the SSI/BiSS-data by providing additional information, for example data from an external multiturn counter or error information.
Configuration of the AM-IPE-NONIUS unit is possible either via USB, SPI- or BiSS- interface through the EEPROM of internal GC-NIP circuit. The unit can be connected via RS422 to a standard counter or control unit. Beside the SPI it is possible to activate the SSI/BiSS mode via USB and connect the unit to a SSI/BiSS master.

2 Features

Table 1: Feature overview

Interfaces	
Analogue input	Sinusoidal / cosinusoidal / reference (index) signals, differential or single-ended Adjustable amplification for 660 mV_{PP} / 250 mV_{PP} / 120 mV_{PP} / 60 mV_{PP} Input frequency max.130 kHz for nonius calculation; max. 90 kHz for interpolation
ABZ	90° square-wave sequences (A/B/Z) Adjustable width of zero signal Z to ¼ or 1 period A/B Error signal; Interrupt signal for external processing Service signals for sensor adjustment
SPI	30-bit counter value for the interpolation channels Up to 22-bit resolution for the absolute position 9-bit sensor status information on each channel Compatible to Standard-SPI: 16-bit, MSB first, up to 15 MHz
SSI and BiSS	Up to 30-bit counter value 2-bit sensor status Gray code / binary code adjustable timing SSI ring operation BiSS up to 10 MHz, SSI up to 5 MHz
Additional inputs	Trigger input for storage of the measured value Preset signal for adjustment and storage of the counter values Reference position alignment using external signal
Configuration options	Integrated EEPROM Configuration inputs Serial Interface (SPI/BiSS)
Interpolation / Nonius calculation / Signal processing	
Interpolation rate	256 to 8192, divisible by 8 Adjustable Divider 1/2/4/8 for the AB-signals on each channel
Nonius pitch	Number of periods per turn for absolute position calculation Interpolation rate / [8 / 16 / 32 / 64]
Nonius correction	Correction coefficients stored in EEPROM Software based calibration process for determination of the correction coefficients
Signal correction	AMAC-specific digital controller for the offset, control range ±10% of the standard amplitude AMAC-specific digital controller for the amplitude, control range 60% … 120% of the standard amplitude Digital potentiometer with 64 steps for phase correction; selectable range ±5° or ±10° Input signal monitoring with configurable error indication
Suppression of disturbances	Adjustable low pass filter 10 kHz, 75 kHz, 150 kHz Digital hysteresis for suppression of the edge noise at the output (configurable 0...7) Selectable minimum edge distance at the output (bandwidth limitation)
Reference signal processing	Adjustable reference mark position in 32 steps 0 … 360° Optional: high precision alignment of the reference mark position (configuration via external signal possible) Processing of distance coded reference marks Measured-value trigger at the reference mark position
Miscellaneous	Optional Master-SPI interface for output and manipulation of SSI/BiSS-Data 2-stage measured value trigger Constant delay between sampling and measurement value for all resolutions
Main features	
Operating voltage	5.0V
Temperature range	-40 … 85 °C
Housing	Miniature aluminium casing 55mm x 100mm x 24mm, IP20, Connector HD-SUB-D 26-pin, mini USB

NOTE: *Further information and detailed descriptions of all features, interfaces and configuration possibilities of the AM-IPE-NONIUS can be found in the data sheet of the AMAC nonius interpolation circuit GC-NIP at www.amac-chemnitz.de.*

3 Interpolation and nonius calculation

The signal periods of the analogue sinusoidal and cosinusoidal signals are divided according to the selected interpolation rate and provided to the serial interfaces (SPI/SSI/BiSS) as phase and count value. In parallel, square-wave sequences with 90° phase shift (A/B/Z signals) are generated.

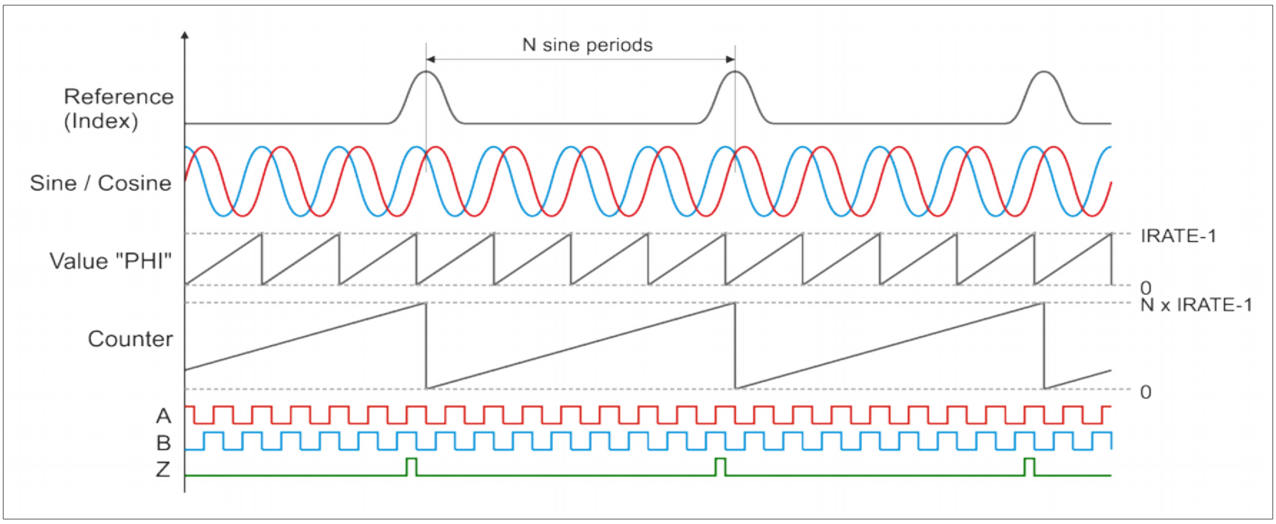


Figure 1: Interpolation

Using the phase values of the two channels and the vernier scale (nonius) method, the absolute position of the sensor is determined on the measuring scale. Errors of the sensor signal or resulting from inaccuracies of the measuring scale can be suppressed by way of an integrated correction. Therefore, 16 correction coefficients, determined by a software-based calibration algorithm, can be stored in the GC-NIP internal EEPROM inside the AM-IPE-NONIUS.

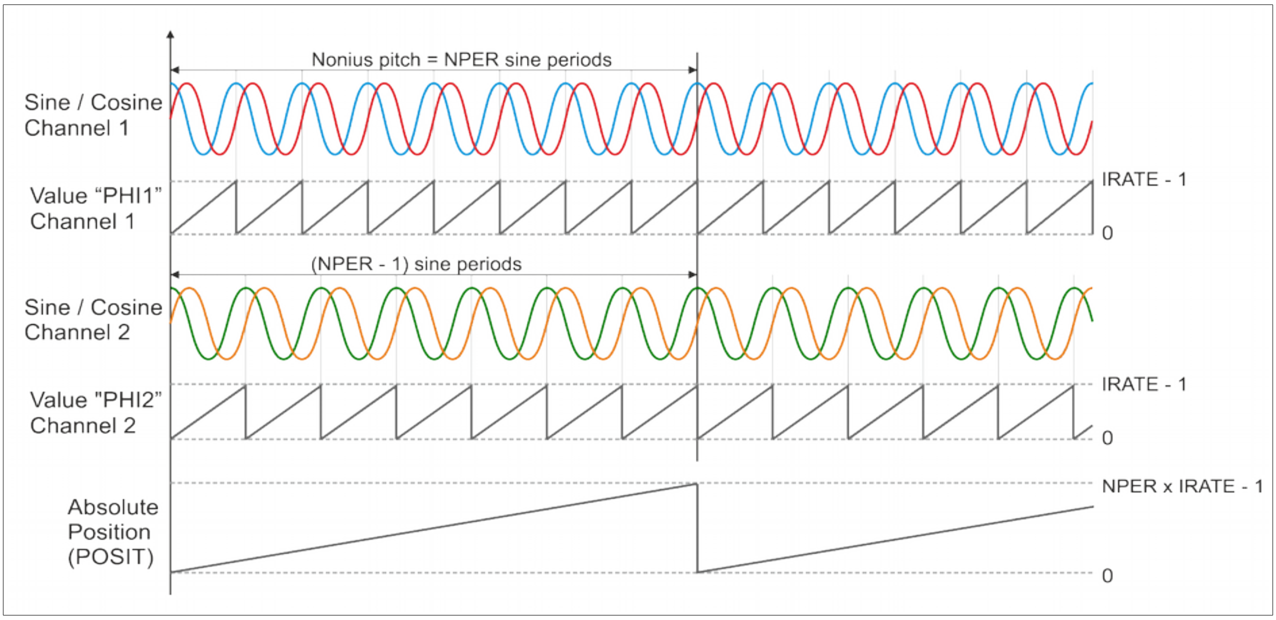


Figure 2: Nonius calculation

Table 2: Operating modes of the GC-NIP

Mode	CFG1/Mode'(3:0)	Sensor type	Measuring values	
Nonius + ABZ	X000	Nonius sensor	Register CNT1: Register CNT2: Register POSIT: SSI/BiSS: ABZ1: ABZ2:	Incremental position channel 1 Incremental position channel 2 Absolute position [1)] Absolute position [1)] Incremental signals channel 1 Incremental signals channel 2
Two channel	X000	2 independent sensors	Register CNT1: Register CNT2: Register POSIT: SSI/BiSS: ABZ1: ABZ2:	Incremental position channel 1 Incremental position channel 2 Incremental position 1 and/or 2 [1)] Incremental position 1 and/or 2 [1)] Incremental signals channel 1 Incremental signals channel 2
Calibration	0101	Nonius sensor	Register CNT1: Register CNT2: Register POSIT: SSI/BiSS: ABZ1: ABZ2:	Incremental position channel 1 Incremental position channel 2 Absolute position [1)] Absolute position [1)] Test signals for sensor adjustment Test signals for sensor adjustment

[1)] The content of register `POSIT` is selected via `CFGBiSS/STSEL(1:0)` (see Register description)

3.1 Interpolation rate and nonius pitch

The term 'interpolation rate' (`IRATE`) is here understood as the number of increments, into which the sinusoidal/cosinusoidal period of the input signals is divided. 'Nonius pitch' describes the number of periods of the input signals, where the absolute position can be clearly assigned using the vernier (nonius) method. Possible interpolation rates for the nonius calculation of the AM-IPE-NONIUS can be selected between 256 and 8192 and must be divisible by 8. Additionally, the interpolation rate for the integrated interpolation counters and the square-wave-signal outputs (A/B) can be divided by a selectable factor (`IRDIV`) of 1, 2, 4 or 8 (both channels independently). The divided interpolation rate of the incremental counters corresponds the number of signal transitions at the A/B outputs per input signal period. The number of square-wave periods at the outputs `A` and `B` amounts to ¼ of the divided interpolation rate. The nonius pitch (`NPER`) is selectable from the values `IRATE/8`, `IRATE/16`, `IRATE/32` or `IRATE/64`.

Following table shows possible combinations and limitations of interpolation rate and nonius pitch for different interfaces and use cases.

Table 3: Selecting interpolation rate and nonius pitch

Interface / use case	Interpolation rate	Requirement/Limitation	Possible values for nonius pitch
Singleturn Nonius	IRATE from EEPROM 256 … 8192	IRATE is divisible by 8	NPER = IRATE / DIV DIV = [8, 16, 32, 64] If DIV = 8: IRATE ≤ 4096
Internal interpolation counter	IRATE from EEPROM / IRDIV IRDIV = [1, 2, 4, 8]	IRATE is divisible by 8	No influence
A/B-Output	IRATE from EEPROM / IRDIV IRDIV = [1, 2, 4, 8] IRDIV2 = [1, 2, 4, 8] (IRD2SEL = 1)	IRATE is divisible by 8 IRATE/IRDIV is divisible by 4	No influence

4 Input signals

The AM-IPE-NONIUS operates with both single-ended and differential input signals. The amplification is identical for all signals of the sensor (sinusoidal, cosinusoidal, index/reference). To adapt the AM-IPE-NONIUS to customized sensors, the mean voltage of the instrumentation amplifiers is provided at pins `V0_CH1` and `V0_CH2` (see table 13).

4.1 Input amplifier

The GC-NIP inside incorporates six instrumentation amplifiers with adjustable gain factors. The instrumentation amplifiers are connected to the internal AD converters. Alternatively, this connection is done directly or via a configurable low-pass filter. The conversion range of the analogue-digital-converter and the reference voltages of the instrumentation amplifiers are pre-adjusted, so that internal offset-error are already compensated. The signals on the input of the analogue-digital-converters can be monitored using the pins `SMON1`, `CMON1`, `SMON2` and `CMON2` (see table 15).

Table 4: Configuration signal amplitude (nominal) (Register `CFG1`)

CFG1/GAIN(1:0)	00	01	10	11
Input voltage for differential supply [1](mV$_{pp}$)	330	125	60	30
Input voltage $U_{DiffNom}$ nominal (mV$_{pp}$)	660	250	120	60
Input voltage range for U_{Diff} (mV$_{pp}$)	400...800	150...300	75...145	36...72
Input voltage for maximal ADC-range $U_{DiffMAX}$ (mV$_{pp}$)	990	375	180	90
Reference voltage on `V0` nominal	1.1	1.1	1.1	1.1
Output voltage U_{MON} nominal on `SMON` / `CMON` (V$_{pp}$)	1.27	1.27	1.27	1.27
Amplification (U_{MON} / U_{DIFF})	1.92	5.08	10.6	21.2

[1] at each of the inputs `SINP`, `SINN`, `COSP`, `COSN`

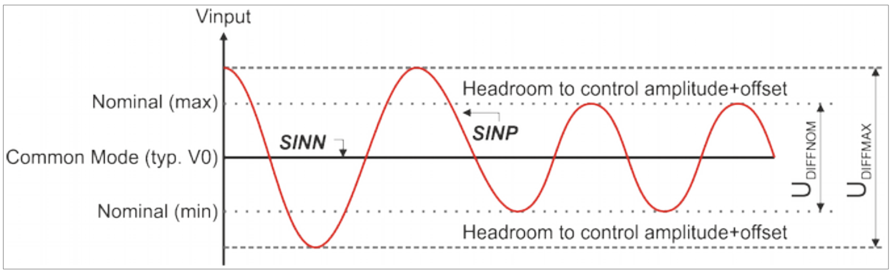


Figure 2: Input signal (single-ended)

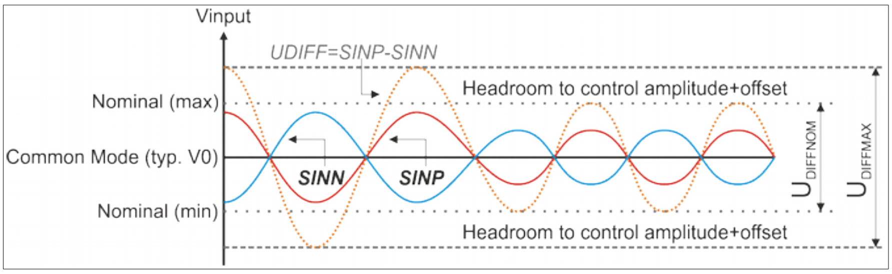


Figure 3: Input signal (differential)

4.2 Signal correction

The input signals are subjected to an AMAC-specific internal gain and offset control. The amplitudes are controlled in the range between 60 % and 120 % of the standard amplitude. The control range for the offset of the two input signals is ± 10 % of the nominal amplitude. The phase displacement of the input signals can be corrected statically in 64 steps using a digital potentiometer. The setting range of the phase is set to approx. +/-5° or approx. +/-10° by way of a configuration bit.

Table 5: Signal correction

Parameter	as a percentage referred to the nominal amplitude (PEAK-PEAK)	as a percentage referred to the ADC-maximum (PEAK-PEAK)	in mV referred to the standard signal (0.66 Vpp)	in V on the pin SMON and CMON (PEAK-PEAK)
Maximal value at the input ($Vmax_{pp}$)	150	100	990	1.90
Nominal value of the input signal ($Vnom_{pp}$)	100	66.7	660	1.27
Guaranteed control range for the amplitude	60... 120	40... 80	400... 800	0.76 … 1.52
Setting range of the amplitude controller	56... 168 [1)]	38... 112 [1)]	370... 1110 [1)]	0.71 … 2.13 [1)]
Vector monitoring[2)]	30	20	200	0.38
Guaranteed control range for the offset (sensor)	±15	±10	±70	±0.133
Setting range of the offset controller	±25	±17	±165	±0.315

1) The setting range for the amplitude is greater than the control range of the ADC.
2) An aggregate signal from sine and cosine is monitored.

4.3 Reference signal / Zero signal Z

The reference signal of measuring systems is typically called Zero signal Z, index point or REF and is detected if the voltage on input pin REFP is bigger than voltage on input pin REFN.
The zero signal Z is generated when the sinusoidal and cosinusoidal analogue signals display a phase angle defined by Parameter ZPOS and at the same time the differential voltage of the reference inputs REFP and REFN exceeds the switching point. The default configuration for the phase angle is set to 45° at manufacturing. The switching points of the reference signal must lie in the range between ZPOS ± [90°...150°]. The width of the zero signal Z at the output can be switched between 1 and 4 increments, i.e. between ¼ and 1 period of the output signals A and B.

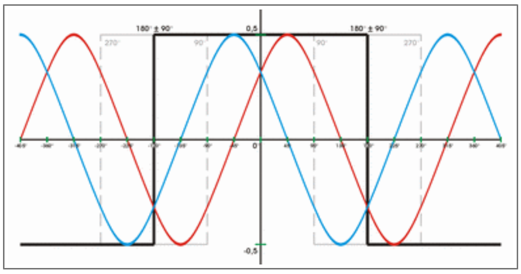


Figure 4: Reference signal

4.4 Maximum input frequency

The maximum input frequency depends on the selected interface at the output. If the square-wave-signals (A/B/Z) are used at the output, the maximum input frequency is limited by the interpolation rate for the AB-signals and the minimum edge interval (tpp). When only using the internal count value through the serial interface, the maximum input frequency is determined by the clock frequency of the circuit (fOSZ). The maximum input frequency for the absolute position calculation (nonius) is limited by the error monitoring for the nonius result (MNON). The error reporting for exceeding the frequency limit is switched by the bit MABZ and MFAST in Register CFG1. Using the square wave signals at the output requires initializing both MABZ and MFAST with '1'. If the serial interface is used and the counters are read, MABZ can be deactivated. For only using the absolute position value via the serial interface, MABZ and MFAST can be deactivated.

Table 6: Maximum input frequency

Mode	MABZ	MFAST	MNON	Max. frequency for nonius calculation	Max. frequency for the counter	Max. frequency for the ABZ output
Nonius	0	0	1	$f_{MAX} \approx f_{OSZ} / 198$	No error detection	No error detection
Counter	0	1	x		$f_{MAX} \approx f_{OSZ} / 280$	No error detection
Square-wave,, $t_{pp} = N/f_{OSZ}$ $N = 2^{CFG1\text{-}TPP(2:0)}$ Interpolation rate ABZ $IRAB = IRATE / 2^{CFG1\text{-}IRDIV(1:0)}$	1	1	x		$f_{MAX} \approx 0.9 \cdot f_{OSZ} / (N \cdot IRAB) < f_{OSZ} / 280$	

4.5 Error monitoring and Status LED

The GC-NIP inside the AM-IPE-NONIUS provides 9 error signals on each channel for the signal monitoring. The sources can be activated or deactivated using the relevant bit in the register CFG1. Storage of the individual error flags can be activated using one further configuration bit each. The OR combination of the error signals saved or masked in this way is provided at the pin NERR (L-active). Additional warnings and error information and the individual error conditions can be read via the serial interface (SPI,SSI,BiSS).

NOTE: *If the error signal has been activated or one of the error bits has been set in the result register, the current measurement result and all subsequent results must be discarded. After rectification of the error cause, the error bits can be reset by command RESCNT or by PRESET impulse. For measurements using a reference mark, it is imperative to pass through the reference point to be able to perform further absolute measurements.*

Table 7: Overview sensor monitoring

NAME	Description	SPI	ABZ	SSI / BiSS
EVLOW	The signal vector generated from sine- and cosine-signal is too small.	Status bit	Error	Error
EADC	One or both A/D converters are overdriven.	Status bit	Error	Error
EOFFS	The offset controller has reached its limit.	Status bit	Error	Warning
EGAIN	The gain controller has reached its limit.	Status bit	Error	Warning
EFAST	The input frequency is too high.	Status bit	Error	Error
EABZ	The Signals `A`, `B` and `Z` are invalid.	Status bit	Error	-
ENON	The nonius calculation result is implausible.	Status bit	Error	Error

The error monitoring is configured by the user by switching the relevant bits in register CFG1. In principle, it is recommended to activate all error signals.

Table 8: Recommended configuration of the error monitoring

	ABZ-Interface	SPI-Interface	SSI-Interface	BiSS-Interface
Activated monitoring bits	EVLOW EADC EOFFS EGAIN EFAST ENON 2) EABZ	EVLOW EADC EOFFS EGAIN EFAST 1) ENON 2) (EABZ) 3)	EVLOW EADC EOFFS EGAIN EFAST 1) ENON 2) (EABZ) 3)	EVLOW EADC EOFFS EGAIN EFAST 1) ENON 2) (EABZ) 3)
Indication in case of error	Error signal on pin `NERR`	Error bit in register `STAT` Error bit in `POSIT` register Error signal at pin `NERR`	2 bits warning and error in the SSI data stream	2 bits warning and error in the BiSS data stream

1) If only the absolute position is used, the frequency monitoring can also be switched off via MFAST.
2) If only used the one- or two-channel interpolation without nonius calculation, the monitoring of the nonius calculation can be switched off via MNON.
3) If not using the square wave outputs `A`, `B` and `Z`, the monitoring of the maximum ABZ-frequency (bit `MABZ`) can be switched off.

The Status LED on top of the AM-IPE-NONIUS lights green if no error occurs and the pin NERR is high. A Low signal (Error state) at the pin NERR turns the Status LED red until the error is set back. The internal Power LED turn green after power on and indicates the AM-IPE-NONIUS is connected properly to the power supply.

Table 9: LEDs

LED	Signal	Meaning
STATUS LED (LD1/LD2)	Red (LD1 off)	An error occurred
	Green (LD2off)	Normal operation
Power LED LD3	Off	Power Off
	Green	Power On

5 Interfaces and Output signals

The AM-IPE-NONIUS runs different output interface modes. The ABZ mode is the normal counter mode with ABZ signals at the outputs for each channel. Parallel an SPI is available for configuration and measurement. In BiSS mode the ABZ outputs at channel 1 change to operate in this Interface mode and can also be used for configuration and measurement. Alternatively this interface can operate at SSI in counter only mode and measured values are available via this interface. In BiSS/SSI mode the SPI is not available. Finally the ABZ outputs at channel 2 can be changed to operate at simple SPI mode which sends the position data (register POSIT) cyclical to a connected slave. The received data of this simple SPI form the bits 31:0 of the SSI- or BiSS-data. In this way additional information from an external multiturn counter or extra error information f.e. can be also transferred. For further information about available interfaces and configutration refer to the latest relaes of the GC-NIP data sheet.
The AM-IPE-NONIUS will be delivered running ABZ mode on both channel with a parallel available SPI, but modes can be configured by USB using the software monitor tool.

For further information about available interfaces and configuration refer to the latest release of the GC-NIP data sheet at www.amac-chemnitz.de**.**

5.1 ABZ output signals

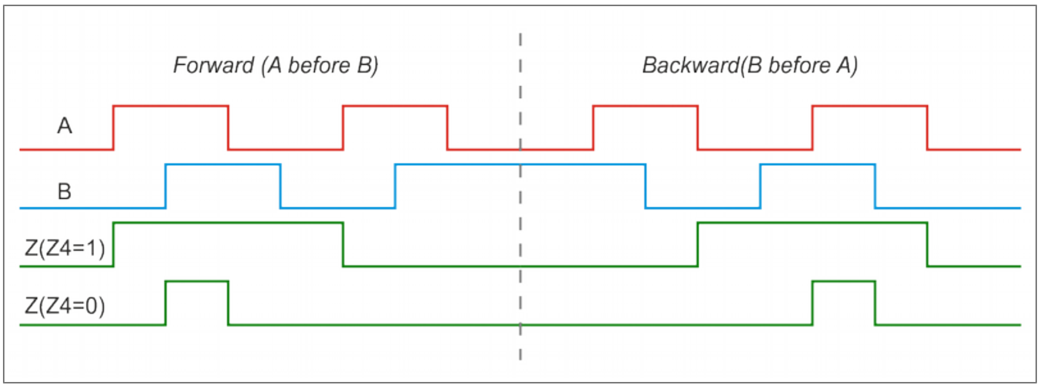


Figure 5: Output signals ABZ

The minimum time interval t_{pp}, at which the output signals `A`,`B` and `Z` may switch, can be adjusted in binary steps between $1/f_{OSZ}$ and $128/f_{OSZ}$ using the edge distance control configuration bits `CFG1/TPP(2:0)`. After switching one of the outputs, the subsequent edge of the other signal will only be visible at the AM-IPE-NONIUS output after the time t_{pp} has elapsed. Thus, in case of a short-time disturbance of the input signals, a subsequent interpolation counter will operate without errors. The configuration of the edge interval t_{pp} depends on the counter connected to `A`,`B` and `Z`. Please note the discretization of time at the output of the AM-IPE-NONIUS due to the edge interval setting. The GC-NIP inside the AM-IPE-NONIUS uses a digital interpolation method. This causes the speed-proportional A/B/Z output signals to be overlaid by the inevitable quantization errors (the so called ±1INK errors) resulting from the A/D converters. The quantization noise can be suppressed by activating the digital hysteresis using register CFG1/DH(2:0). This prevents switching of the outputs with static input signals. In this case, all output signals are delayed by one increment.

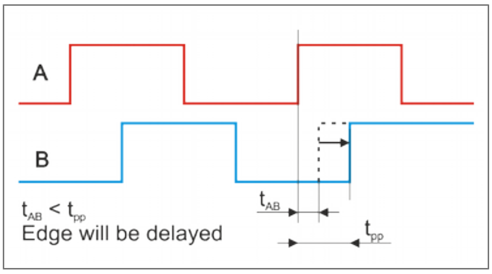


Figure 3: Edge interval setting

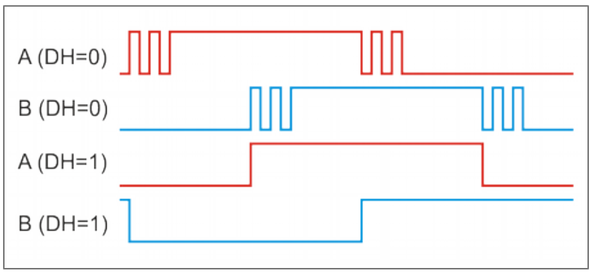


Figure 4: Digital hysteresis

5.2 Serial interface SPI

The serial interface SPI operates in slave mode and is activated by default factory settings. Up to sixteen AM-IPE-NONIUS can be operated on a single interface bus. The interface is compatible to the most important microcontroller families in SPI mode 0 (16 bit data, MSB first, SCK default low, sampling with rising clock signal edge).

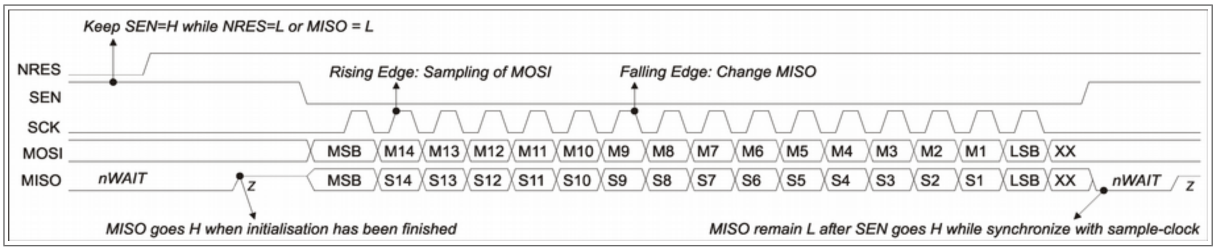


Figure 6: SPI timing diagram

OP-Code	Description	Bit at signal MOSI															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		OPC				HWA				DATA							
WRA	Write address	1	0	0	nB	H3	H2	H1	H0	A7	A6	A5	A4	A3	A2	A1	A0
WRD	Write data	1	0	1	nB	H3	H2	H1	H0	D7	D6	D5	D4	D3	D2	D1	D0
RD0/ST	Read Bytes 0+1 (2 LSB)	1	1	0	X	H3	H2	H1	H0	A7	A6	A5	A4	A3	A2	A1 *)	0
RD1	Read Bytes 2+3 (2 MSB)	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X
NOP	Output read register	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

`H(3:0)`: Hardware address, default: '0000', Is not evaluated if `nB` = 0
`A(7:0)`: Register address within an IC
`D(7:0)`: Data word / write data (read data will appear at the pin `MISO`)
`nB`: Broadcast (L-active) 0: Command to all ICs
1: Command to the IC addressed by way of `H(3:0)`

Register access is done by writing 8 bit and reading 16 bit. The registers are organized by way of 32 bit blocks. Therefore, the IC contains a 32 bit holding register for read access. Data to be read is stored in the holding register using the SPI word `RD0/ST`. The two least significant bytes of the data to be read is output at the pin `MISO` during the **next** SPI access. The two most significant bytes of the read access are output with the SPI cycle following the command `RD1`. To read a 32 bit register, the commands `RD0/ST`, `RD1` and `NOP` are usually executed one after another. To read several registers in succession, the sequence `RD0` – `RD1` – `RD0` – `RD1`... can be used.

To write a register, first the register address must be set using the SPI word `WRA`. Subsequently, the register can be programmed using `WRD`. The register is programmed byte by byte.

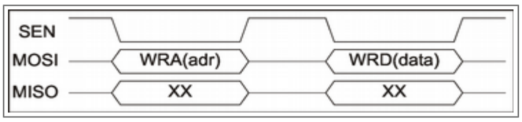


Figure 7: Write access 8 Bit

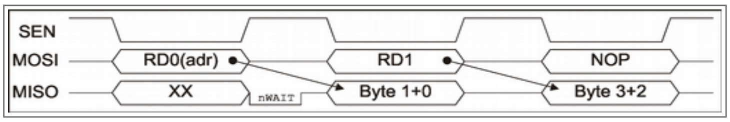


Figure 8: Read access 32 Bit

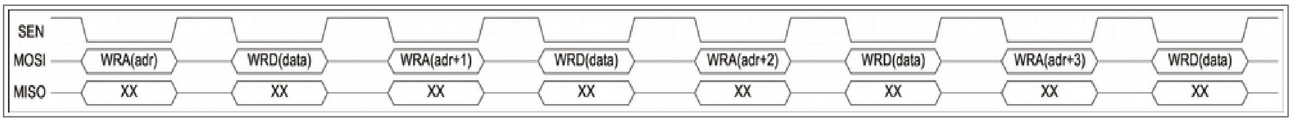


Figure 9: Write access 32 Bit

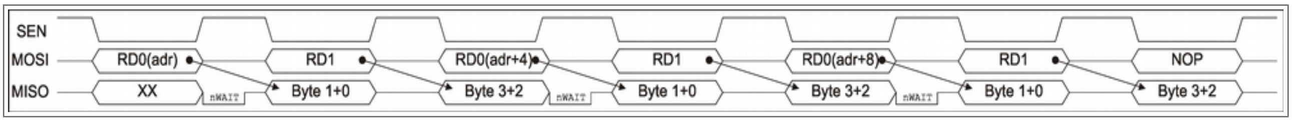


Figure 10: Read access 3 x 32 Bit

5.3 BiSS Interface

The Single Cycle Data (SCD) transferred in BiSS C-mode contains the actual position value from register `POSIT` with an overall length of 40 bit. This includes the 32 bit position, two bits of error information (error and warning bit) and the CRC checksum (polynomial 0x43, 6 bit, inverted).

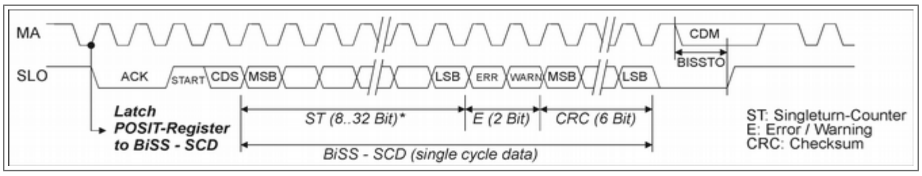


Figure 11: BiSS SCD (Single Cycle Data)

Using the BiSS register access, all registers of the GC-NIP inside the AM-IPE-NONIUS are attainable. Reading of 32 bit registers requires the bit `READ32` in register `CFGBISS` to be set. Read access is then handled in 32 bit format, so 4 subsequent addresses, beginning with the least significant address (divisible by 4), must be read by the master.

Table 10: Default values BiSS register

Register	Vendor configuration	User configuration
BiSS serial number	MSB: 0 LSB: level at pins `HWA(3:0)`	MSB: unique serial number LSB: level at pins `HWA(3:0)`
BiSS Vendor ID	0x47 0x43 („GC“)	User defined ID
BiSS Device ID	0x32 0x03 0x00 0x00	User defined ID
BiSS-Profile + Electronic data sheet (EDS)	unused	User profile

Further specification of the BiSS interface, signal waveforms, register description as well as information to the electronic data sheet (EDS) can be found on the website www.biss-interface.com.

5.4 SSI Interface

The SSI data output contains the position value with an overall length of 20 or 32 bit. This contains the measured position and two bits of error information (error and warning). Setting the SSI to Ring Mode enables continuous transmission of the measurement value.

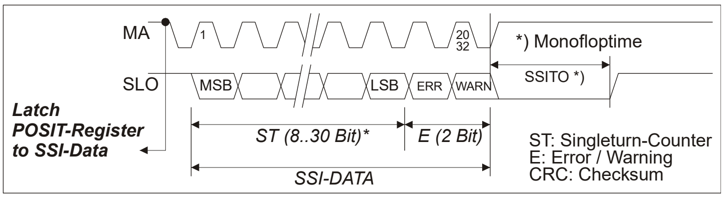


Figure 12: SSI

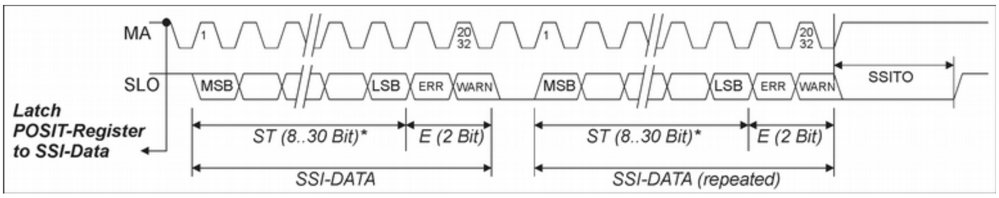


Figure 13: SSI (Ring mode)

6 Characteristic values

Table 11: Characteristic values

Operating conditions	**Min.**	**Nom.**	**Max.**	**Unit**
Operating voltage	4.5	5.0	5.5	V
Current consumption				mA
Output voltage at $SVCC_x$		3.3 / 5.0		V
Output current at SVCCx				mA
Output voltage at V0_CHx		1.1 / 2.5		V
Output current at V0_CHx			20	mA
Operating temperature	-40		+85	°C
Input section	**Min.**	**Nom.**	**Max.**	**Unit**
Input frequency (nonius calculation)	0		150	kHz
Input frequency (interpolation)	0		90	kHz
Phase shift between SIN and COS		90		°
Amplitude SINN ⇔ SINP / COSN ⇔ COSP	36	660	800	mV_{pp}
Phase correction	4.5 / 9	5 / 10	9 / 11	°
Oscillator frequency f_{osz}	4		26	MHz
Interpolation	**Min.**	**Nom.**	**Max.**	**Unit**
Interpolation rate (nonius calculation)	256		8192	Increments
Interpolation rate (ABZ)	32		8192	Increments
Minimum interval time t_{pp} A / B signal	$1/f_{OSZ}$		$128/f_{OSZ}$	ns
Interpolation accuracy				
Delay time 'Analogue input to nonius result'		$181/f_{OSZ} + 100$		ns
Delay time (A / B / Z)		$208/f_{OSZ} + 100$		ns
SPI Clock frequency			15	MHz
SSI Clock frequency @ $f_{OSZ} \geq 20$MHz			5	MHz
BiSS Clock frequency			10	MHz
Other characteristics	**Housing made of extruded profile**			
Degree of protection	IP20			
Connectors	HDSUB-D, 26-pin			
Dimensions	55 mm x 100 mm x 24 mm			

7 Factory Configuration

The AM-IPE-NONIUS can be matched to most varied measuring systems and subsequent electronic systems by way of the configuration registers. If the IPE is initialized using the integrated GC-NIP EEPROM. The table below provides an overview of the default configuration of the AM-IPE-NONIUS.

Table 12: Default configuration

Configuration	Parameter	Default (EEPROM with factory settings)
Analogue	Phase correction Low pass -1dB Nominal signal amplitude Power saving options	0° 150 kHz 660 mVpp inactive
Interpolation Nonius	Interpolation rate Controller Controller start values Reference mark position Nonius pitch Correction Count direction Power saving options	8000 active, timing 01 Average at 45° 125 none configured via pin DIR inactive
Output signals	Mode TPP Digital hysteresis Z Output in case of error Power saving options	ABZ 0 1 active, 1 increment Hold inactive
Error processing	Error monitoring Error storage	all errors inactive
Special functions	Preset (Nonius) Preset values Nonius offset Trigger pulse edge	Inactive 0x00 0x00 falling
Interface	ABZ SPI interface SSI interface BiSS interface	enabled enabled disabled disabled

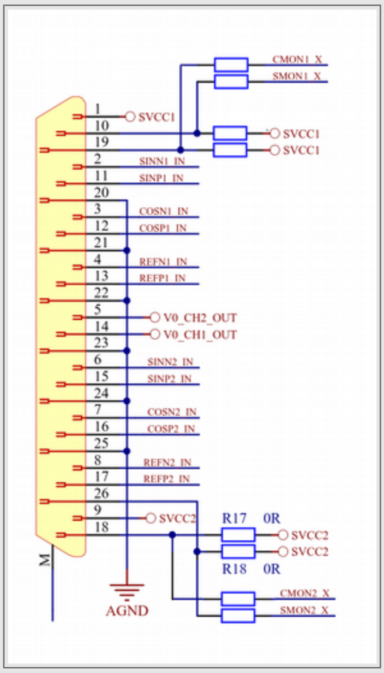
NOTE: *The detailed description of the configuration register set can be found in data sheet of the GC-NIP at www.amac-chemnitz.de.*

8 Configuration of the connectors

8.1 Input connector – X2

Table 13: Input connector – X1 pin assignment (SUB-D 26pin female)

Pin	Name	Signal	Meaning
1	SVCC1	PO	sensor supply voltage channel 1 (default 5V) 3.3V or 5V selectable via connector X6
2	SINN1	AI	negative sine signal channel 1
3	COSN1	AI	negative cosine signal channel 1
4	REFN1	AI	negative reference signal channel 1
5	V0_CH2	AO	V0 – buffered mean voltage channel 2
6	SINN2	AI	negative sine signal channel 2
7	COSN2	AI	negative cosine signal channel 2
8	REFN2	AI	negative reference signal channel 2
9	SVCC2	PO	sensor supply voltage channel 2 (default 5V) 3.3V or 5V selectable via connector X6
10*	<u>SMON1</u> SVCC1	AO PO	sine monitor output at instrumentation amplifier channel 1 sensor supply voltage channel 1 (see description pin 1)
11	SINP1	AI	positive sine signal channel 1
12	COSP1	AI	positive cosine signal channel 1
13	REFP1	AI	positive reference signal channel 1
14	V0_CH1	AO	V0 – buffered mean voltage channel 1
15	SINP2	AI	positive sine signal channel 2
16	COSP2	AI	positive cosine signal channel 2
17	REFP2	AI	positive reference signal channel 2
18*	<u>CMON2</u> SVCC2	AO PO	cosine monitor output at instrumentation amplifier channel 2 sensor supply voltage channel 2 (see description pin 18)
19*	<u>CMON1</u> SVCC1	AO PO	cosine monitor output at instrumentation amplifier channel 1 sensor supply voltage channel 1 (see description pin 1)
20	VSS	P	Ground
21	VSS	P	Ground
22	VSS	P	Ground
23	VSS	P	Ground
24	VSS	P	Ground
25	VSS	P	Ground
26*	<u>SMON2</u> SVCC2	AO PO	sine monitor output at instrumentation amplifier channel 2 sensor supply voltage channel 2 (see description pin 18)
M	Shield	-	Shield

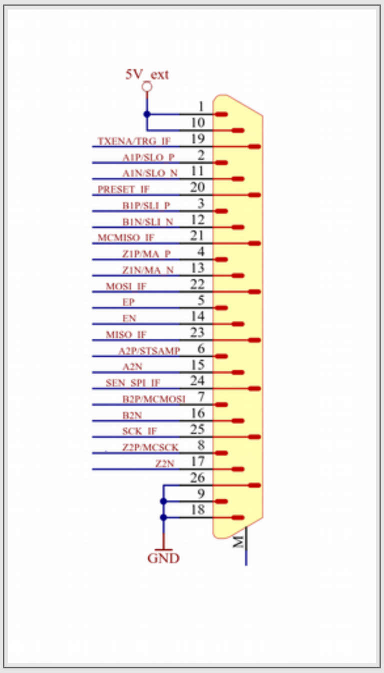


P = power supply, PO = power supply output, AI = Input Analogue, AO = Output Analogue, DI = Input Digital, DO = Output Digital
* default as monitor output (underlined), selectable only via smd resistor assembly

8.2 Output connector – X2

Table 14: Output connector – X2 pin assignment (SUB-D 26-pin male)

Pin	Name	Signal	Meaning
1	5V_ext	P	Supply voltage +5.0V
2	A1P/ SLO_P	DO DO	Incremental Output A channel 1 positive BiSS/SSI: data out positive
3	B1P/ SLI_P	DO DO	Incremental Output B channel 1 positive BiSS/SSI: data in positive
4	Z1P/ MA_P	DO DI	Reference Output Z channel 1 positive BiSS/SSI: clock positive
5	EP	DO	Error Output E positive
6	A2P/ STSAMP	DO DO	Incremental Output A channel 2 positive Controller interface – sync signal
7	B2P/ MCMOSI	DO DO	Incremental Output B channel 2 positive Controller interface – data out
8	Z2P/ MCSCK	DO DO	Reference Output Z channel 2 positive Controller interface – clock
9	VSS	P	Ground
10	5V_ext	P	Supply voltage +5.0V
11	A1N/ SLO_N	DO DO	Incremental Output A channel 1 negative BiSS/SSI: data out negative
12	B1N/ SLI_N	DO DI	Incremental Output B channel 1 negative BiSS/SSI: data in negative
13	Z1N/ MA_N	DO DI	Reference Output Z channel 1 negative BiSS/SSI: clock negative
14	EN	DO	Error Output E negative
15	A2N	DO	Incremental Output A channel 2 negative
16	B2N	DO	Incremental Output B channel 2 negative
17	Z2N	DO	Reference Output Z channel 2 negative
18	VSS	P	Ground
19	TXENA/ TRG	DI DI	Controller interface enable / Trigger
20	PRESET	DI	Input for the preset function
21	MCMISO	DI	Controller interface – data in
22	MOSI	DI	SPI: data in
23	MISO	DO	SPI: data out
24	SEN_SPI	DI	SPI: select / during Reset: select interface SPI / BiSS or SSI
25	SCK	DI	SPI/BiSS/SSI Clock
26	VSS	P	Ground
M	Shield	-	Shield



P = power supply, PO = power supply output, AI = Input Analogue, AO = Output Analogue, DI = Input Digital, DO = Output Digital
* default as monitor output (underlined), selectable only via smd resistor assembly

8.3 Sine/Cosine monitor connectors – X3/4 (inside the case)

Table 15: Sine/Cosine monitor connectors – X3/4 pin assignment (1.27mm 6 Way 2 Row Header Pin)

Pin	Name	Signal	Meaning
1	GND	Output	Analogue ground for measurements
2	CMONx	Output	Test signal of the cosine channel x of the analogue input stage
3	GND	Output	Analogue ground for measurements
4	SMONx	Output	Test signal of the sine channel x of the analogue input stage
5	GND	Output	Analogue ground for measurements
6	V0CHx	Output	V0 voltage

8.4 Sensor voltage selector – X5/6 (inside the case)

Table 16: 8.4 Sensor voltage selector – X5/6 pin assignment (2.54mm 3 Way Header Pin)

Pin	Name	Signal	Meaning
1	5V	Power	
2	SVCCx	Output	
3	3.3V	Power	

8.5 USB interface - X10

Table 17: USB interface – X10 pin assignment

Pin	Name	Meaning
1	+ USB	+ 5 V
2	USBD -	Data -
3	USBD +	Data +
4	ID	–
5	- USB	GND

9 Software – NIP-Monitor

The NIP-Monitor-Software allows to visualise and control the parameters and characteristics of the AM-IPE-NONIUS over USB. Furthermore, the active interfaces ABZ/SPI/SSI/BiSS at the output connector can be selected by this program. The Software is designed for Windows operating systems and available for download on our website **www.amac-chemnitz.de**.

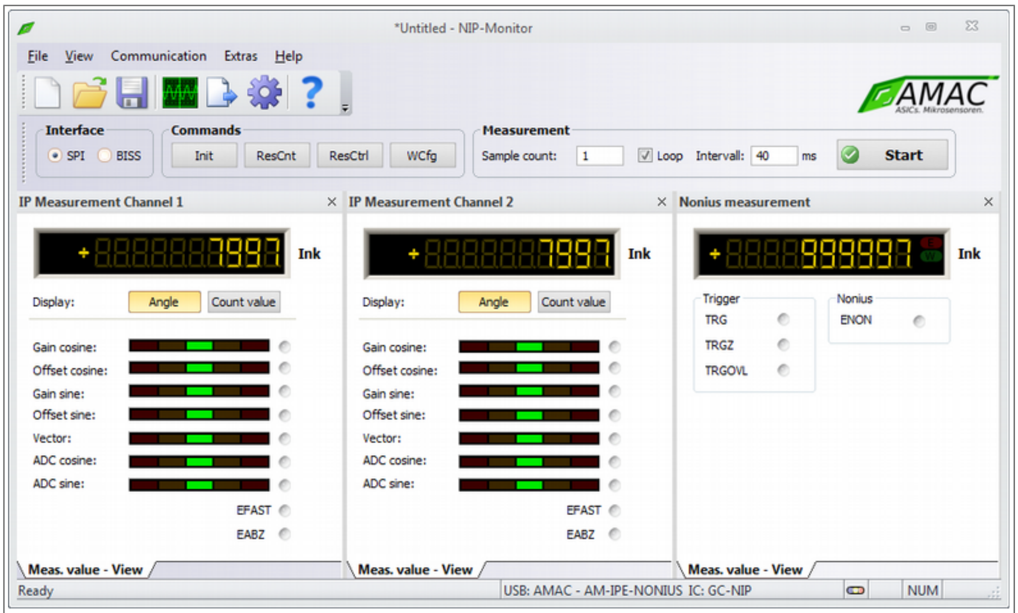


Figure 14: Software NIP-Monitor

10 Hardware overview

10.1 Connections and test points

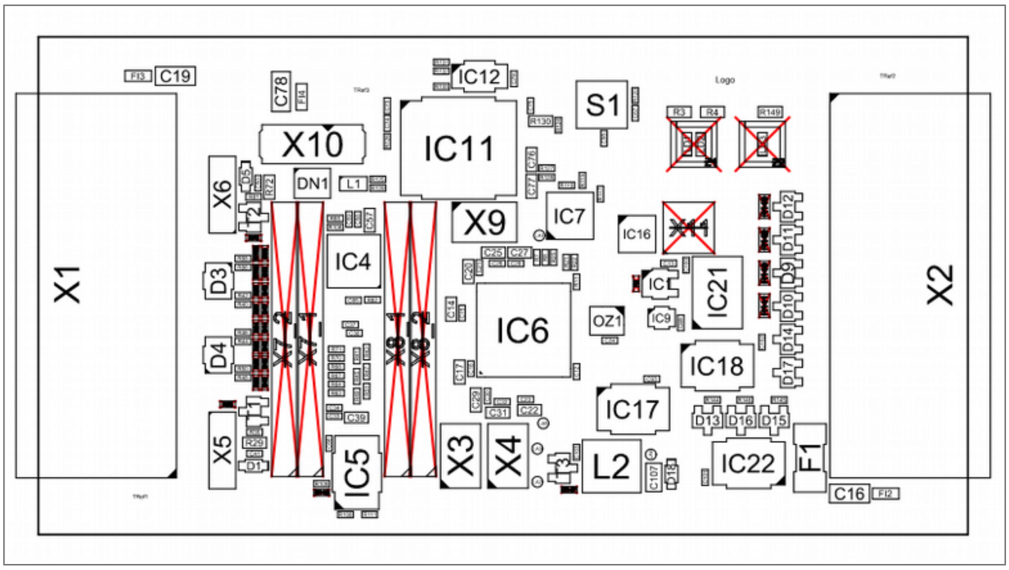


Figure 15: Connections and test points

10.2 Dimensions

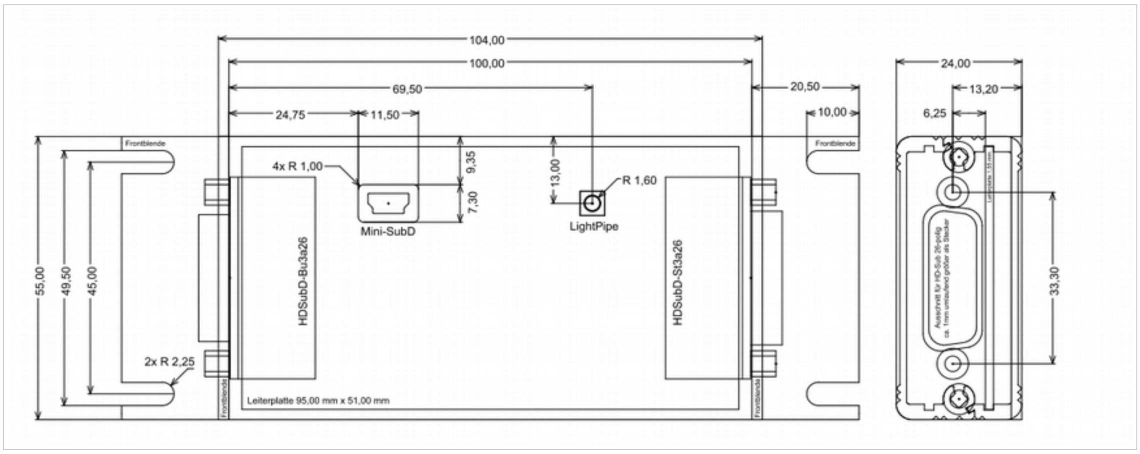


Figure 16: Dimensions

10.3 Accessories (optional)

10.3.1 Test adapters

These two test adapter are designed for evaluation purposes of AM-IPE-NONIUS. Adapter 1 can be used for sensor connections and provides two standard 15 pol SUB-D connectors and several pin stripes. So it is easy to connect sensors to AM-IPE-NONIUS and makes it possible to observes the sensor signals through the pin stripes.
Adapter 2 can be used as an easy way to connect the different output interfaces over separate pin stripes for each interface to AM-IPE-NONIUS. In addition two standard 15 pol SUB-D connectors are also provided for a direct connections to f.e. standard counters. Then it's also possible to monitor interface traffic and detect communication errors through pin stripes.

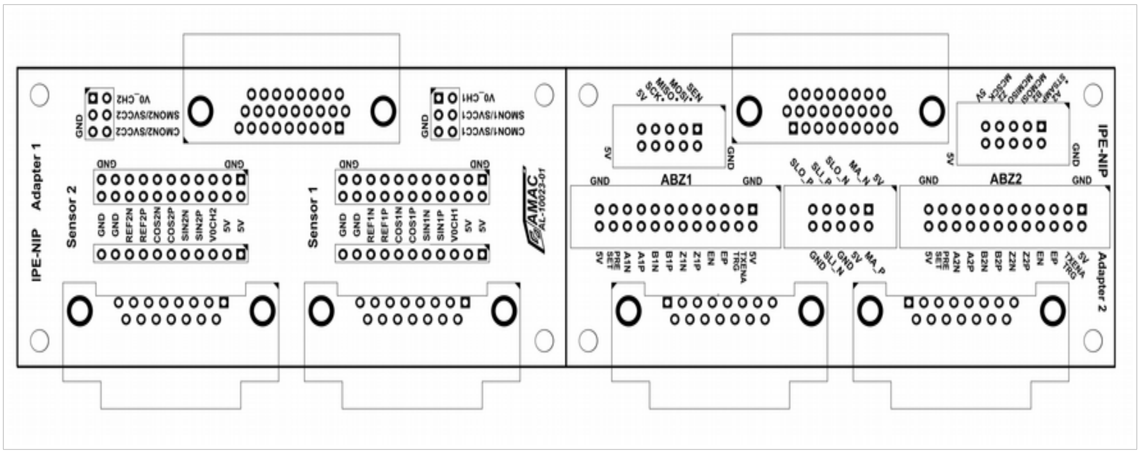


Figure 17: Test adapters

11 Ordering information

Table 18: Ordering information IPE4k

Product type	Description	Article number
AM-IPE-NONIUS	Nonius Interpolation unit with GC-NIP (Standard configuration ABZ)	PR-44820-00
AM-IPE-NONIUS-TB	Two test adapters for evaluation purposes (SUBD Connector X1/X2)	On Request

12 Notes