AM-IP4k

Datasheet

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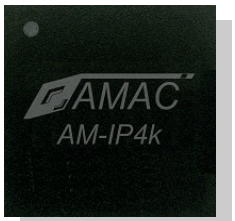

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Revision History

Date	Revision	Change(s)
09/03/2018	1.0	First Version
07/07/2018	1.1	At 2 Features Analogue input range 220 kHZ Figure 1 Block diagram ink word changed to inc. Figure 2 Functional block diagram ink word changed to inc. Overview. Switching analogue filter deleted and modified to low-pass. Figure 4 Input signals (single-ended) update. U to V. Figure 5 Input signals differential update. U to V. Figure 11 Reference signal MVAL(ZMODE) updated to CFG3/ZMODE 01 Figure 21 Mnimum circuit of the AM-IP4K added Table 1: Pin assignment AM-IP4k QFN56 Pin assignment, revised Instrument amplifier changed to instrumentation amplifiers 7.2.2 Phase adjustment added Formula 1 phase adjustment added Formula 2 added Table 5 configuration options CFG2/IRDIV2 added at Interpolation rate. corrected: CFG4/ZPOS2, CFG2/TRGSLP, CFG2/TEAN CFG3 / PHRENA added at phase correction CFGSSI / SSI20 corrected Table 6 at CFG2/TEAN corrected Table 11: Register “Correction” DISKSC 0x013 [1] changed to 0x013 [2] and 0x09[9] changed to 0x09[10] DISK360 0x013 [2] changed to 0x013 [1] and 0x09[10] changed to 0x09[9] 7.4.1 Interpolation rate. Basic interpolation rates described. 7.6 In text 6 possibilities corrected to 7 possibilities At 7.6.1 Sources of error. Correction error see chapter 7.5 changed to 7.7.4 At 7.8 Measured Trigger value Timer high range changed from $22^{24}/f_{OSZ}$ to $22^{16}/f_{OSZ}$ Table 18: ABZ modes (Register CFG1) modified mode 110 deleted. Table 24Commands/Control signals CFG2/TEAN corrected Table 20: Sensor adjustment at Phase adjustment, activate controller corrected. Figure for Duty Cycle /=50 and PHI > 45 swaped with Duty Cycle = 50 and PHI = 45 Register STAT/ID/REV updated. ASICID and ASICREV relocated Register CFG1 description IR [4:0] reset value length 00000 Register CFG2 IRDiv2 bit (7:5) added Register CFG3 DISZ reset value changed to 0 Register CFGSSI CFGSSI / SSI20 corrected Register CFGLDR D(6:0) reset value 0000000 corrected. Table 35 Figure 6 corrected at CMIR to Figure 9 Figure 31 Procedure sequence for EEPROM read/write included in english and divided into two Figures Procedure sequence for EEPROM read and Procedure sequence for EEPROM write
15/01/2020	1.2	Deleted error from non-existing reference. Page 8.
05/02/2020	1.3	Table 18: ABZ modes (Register CFG1) modified, mode 110 deleted. At Features Basis Interpolation rate 2560 added. At Register CGFG2 TEAN to TEAEN changed. Pin assignment V1P1, VRH, VRM, and VRL as AO corrected.

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1 Overview

The interpolation circuit AM-IP4k serves to increase the resolution of incremental position and angular measuring systems with sinusoidal output signals offset by 90°. The input signals are subjected to an AMAC-specific internal gain and offset control, which automatically leads to a correction of amplitude and zero position. Additionally correction of concentricity errors as well as signal form errors are integrated. Furthermore the phase deviation of the input signals can be corrected statically via a digital potentiometer. By dividing the signal period up to 4096 times a position or angle value is calculated and then transferred to following components via a fast SPI interface, a SSI interface, or via standard ABZ square wave signals.

The interpolation circuit AM-IP4k is suitable for both input and output interfaces with 3.3V. It comprises three instrumentation amplifiers with adjustable gain factors. Sensors with voltage interface as well as measuring bridges can be connected directly to this interpolation IC. Sensors with current interface and photodiode-arrays are adapted by a simple external circuit. The AM-IP4k can be used with both single-ended and differential signals. The noise of the sensor signals is reduced by a configurable low-pass filter. Additionally, a digital hysteresis can suppress the edge noise of the output signals at low input frequencies and at standstill. Thus, a consecutively connected interpolation counter works properly even in case of short-time disturbances. The quality of the signals issued by the sensors is monitored in the IC. For that purpose it is possible to activate 6 sources separately, which are producing an error signal.

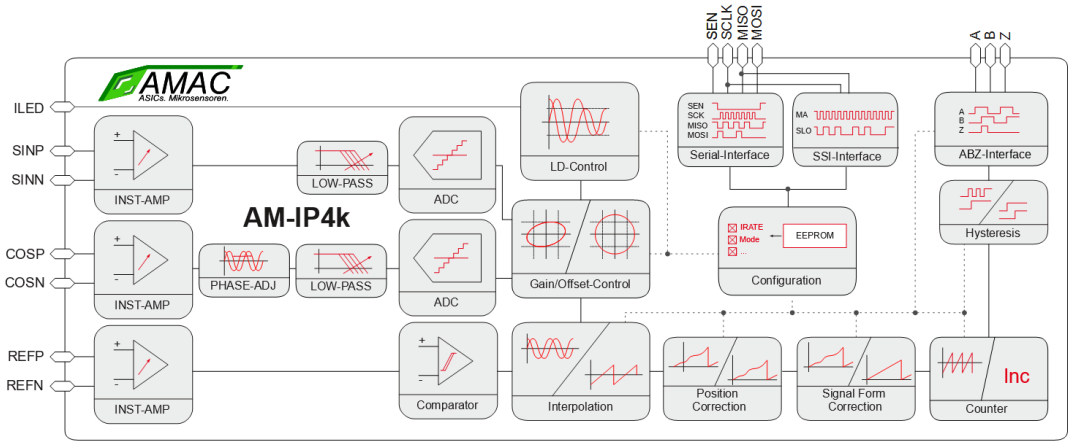


Figure 1: Block diagram

The integrated output signal interfaces (ABZ, SPI, SSI) and further features like an integrated multi-turn counter, the processing of distance coded reference marks, the possibilities of reference point adjustment and zero point adjustment and storage make the IC suitable for direct use in industrial control systems. Furthermore the IC can be used in absolute positioning measuring systems. For optical sensors a controlled current output is provided to control a laser diode. The IC's configuration depends on the specific application and is carried out via an internal EEPROM, configuration pins or serial interface (SPI).

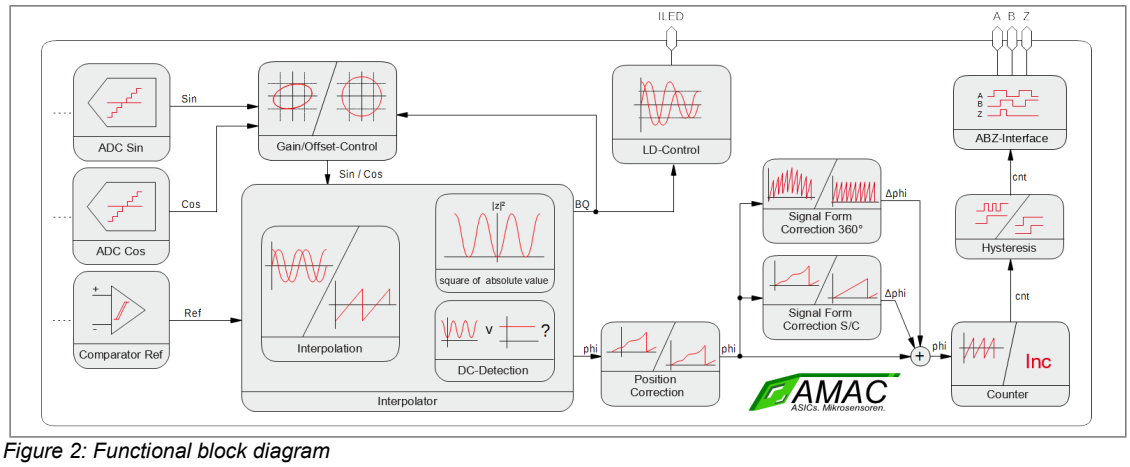


Figure 2: Functional block diagram

2 Features

Interfaces	
Analogue input	- Sine- / Cosine- / Reference signal: differential or single-ended - Nominal amplitude configurable to 1 V_{pp} / 500 mV_{pp} / 250 mV_{pp} / 75 mV_{pp} - Maximum input frequency up to 220 kHz
ABZ	- 90° square wave sequences (A/B/Z) - Adjustable width of the index signal Z of ¼ or 1 period A/B - Error signal - Interrupt signal for µC - Additional signals for sensor adjustment
SPI	- 30 bit count value / 16 bit multi-turn value - Data rate up to 500,000 measured values/s - 9 bit signal monitoring - Compatible with standard SPI: 16 bit, MSB first, up to 25 MHz - Signal filter for noise suppression, configurable
SSI	- SSI 20 bit or 32 bit - 2 bit signal monitoring - Gray code / binary code - Adjustable timing - SSI ring mode
Other inputs	- Trigger signal for measured value storage - Zero signal and teach signal for sensor's zero point adjustment and storage
Current output	- Controlling a laser diode for optical sensors - Controlled by square of the input signals' absolute value - Set current adjustable in 256 steps
Configuration options	- Internal EEPROM - Serial SPI interface
Interpolation / Signal processing	
Interpolation rates	- Interpolation basis rate: 4096, 4000, 3200, 2560[1)] - Configurable divider: 1, 2, 4, 8, 16, 32, 64, 128 additionally for basic IR 4096 (256, 512, 1024) - Interpolation rate adjustable at will via EEPROM table, default setting: 2560[1)]
Signal adjustment	- AMAC-specific digital controller for the offset, control range ±10% of the nominal amplitude - AMAC-specific digital controller for the amplitude, control range 60% … 120% of the nominal amplitude - Digital potentiometer with 64 steps for phase correction; setting range ±5° or ±10° - Input signal monitoring with configurable error indication
Signal correction	- Wobble correction for periodic errors over 360° (rotary encoder) - Signal form correction for periodic errors within one sine/cosine period (for linear encoder too) - Can be activated or deactivated separately
Interference suppression	- Adjustable low-pass filter (Cut-off frequencies 10 kHz, 75 kHz, 250 kHz) - Digital hysteresis to suppress output edge noise - Adjustable minimum edge separation (band width limitation) at the output
Reference signal processing	- Adjustable reference position 0 … 360° - Definition of the optimal reference position via SPI or additional signals - Processing of distance coded reference marks - Measured value trigger at the reference position
Other	- 2-stage measured value trigger - Programmable timer (3.2 µs … 420 ms) - Constant delay between sampling and measurement for all resolutions (at 40 MHz): without signal correction 2.35 µs; with signal correction 3.95 µs - Multi-turn counter
Main features	
Package	QFN56 (8 x 8 mm)
Operating voltage	3.3 V
Temperature range	-40 … +125°C
Interface clock frequency	SPI 25 MHz, SSI 5 MHz

3 Ordering information

Product type	Description	Article number
AM-IP4k	Interpolation circuit AM-IP4k, QFN56	PR-50400-10
USB to SPI Adapter	USB adapter for SPI interface	PR-44025-10

4 Application overview

Signal form (Sensor)	Application of AM-IP4k
Sinusoidal, voltage	Direct connection of AM-IP4k to sensor
Sinusoidal, current	Additional resistors required
Reference (index) track	Direct connection of AM-IP4k to sensor
Square wave	IC not suitable in principle
Signal specification (sensor)	**Application of AM-IP4k**
75mV$_{pp}$ nominal	Direct connection of AM-IP4k to sensor
250mV$_{pp}$ nominal	Direct connection of AM-IP4k to sensor
500mV$_{pp}$ nominal	Direct connection of AM-IP4k to sensor
1 V$_{pp}$ nominal	Direct connection of AM-IP4k to sensor
2 V$_{pp}$ nominal	Additional resistors required
Differential signal, DC reference voltage	Direct connection of AM-IP4k to sensor
Single-ended, DC reference source inside sensor	Direct connection of AM-IP4k to sensor
Single-ended, no DC reference source inside sensor	Direct connection of AM-IP4k to sensor or need for additional resistors
Photo diodes 0.5 µA$_{pp}$	Additional resistors required
Photo diodes 11 µA$_{pp}$ ...16 µA$_{pp}$	Additional resistors required
Resistive measuring bridge (Magnetic sensors)	Direct connection of AM-IP4k to sensor
Fluctuating amplitude of the sensor	AM-IP4k contains a controller for amplitudes
Offset at sensor not correctable	AM-IP4k contains a controller for offsets
Phase at sensor not correctable	AM-IP4k contains a potentiometer for phase adjustment
Variable reference signal position	AM-IP4k provides the possibility for reference point adjustment
Distance-coded reference marks	Special trigger mode for AM-IP4k when connected via SPI
Maximum signal frequency	
Rotary encoders:	f_{max} = (revolution / minute)·(signal periods / revolution) / 60
Linear encoders:	f_{max} = (v_{MAX} [in m/s] / (signal period [in mm]) · 1000
f_{max} < 220 kHz	All interpolation rates up to 4096 via SPI/SSI
f_{max} < 40 MHz / Interpolation rate	For use of the ABZ output
Maximum counter frequency at ABZ is known	Adjustment of AM-IP4k possible via `CFGTPP`
Subsequent electronics	
Output to µController/DSP/FPGA	Connection via SPI interface
Output to external interpolation counter	Connection via ABZ interface
Output to industrial control	Connection via SSI or ABZ interface
System contains several channels	Simultaneous use at a single SPI/SSI bus possible
Real-time application / Equidistant sampling	Constant delay of 2.4 µs (4.0 µs with activated signal correction), use trigger or timer
IC configuration	Internal EEPROM, all registers configurable via SPI
Signal specification LVCMOS	Inputs/Outputs can be used directly
Signal specification RS-422	Line driver required
Limited size	
Package	QFN56, outer dimensions 8 mm x 8 mm
Minimum circuit	See figure 21 • 8 Block-C • 3 pull-up resistors (NRES, NERR, MISO) • 1 pull-down resistor (CLKSEL) • VDD analogue, VDD digital

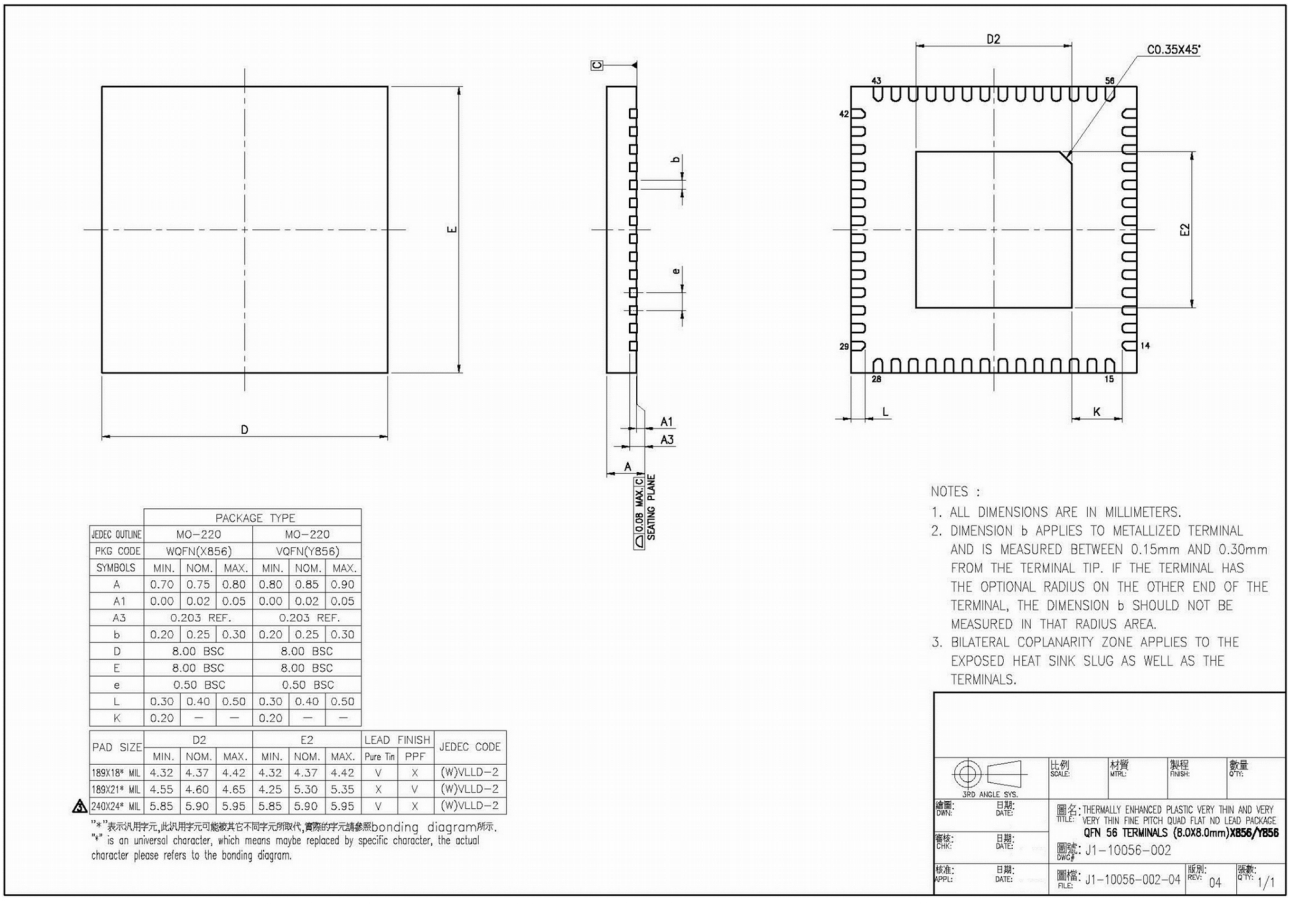
5 Pin assignment

Table 1: Pin assignment AM-IP4k QFN56

Pin no.	Name	Type	Function	Std. value
1	SINP	AI	Quadrature signal 1 – Sine positive	
2	SINN	AI	Quadrature signal 1 – Sine negative	
3	COSP	AI	Quadrature signal 2 – Cosine positive	
4	COSN	AI	Quadrature signal 2 – Cosine negative	
5	REFP	AI	Reference signal positive	
6	REFN	AI	Reference signal negative	
7	V5V	AP	Supply voltage analogue (Mean voltage single-ended)	5.0 V
8	VSS	DP	Digital GND	GND
9	VDD	DP	Supply voltage digital	3.3 V
10	CLK_CLKSEL	DI	Clock selection/Clock input	
11	TM2	DI	Test mode 2	
12	TM	DI	Test mode	
13	TST_0B	DO	Digital test output B, configurable	
14	TST_0A	DO	Digital test output A, configurable	
15	MOSI_SLI	DI	SPI/SSI – Data input	
16	SEN	DI	SPI Enable/Select interface during reset (Chapter 6.1)	
17	SCK_MA	DI	SPI/SSI – Clock	
18	NSS	DO	SPI/Slave Select (SPI Master Mode)	
19	MISO_SLO	DO	SPI/SSI – Data output	
20	NERR	DO	Error, low active	
21	VSSO	DP	Digital GND (I/O)	GND
22	VDDO	DP	Power supply voltage digital (I/O)	3.3 V
23	A	DO	Square wave channel 1	
24	B	DO	Square wave channel 2	
25	Z	DO	Square wave reference/ index	
26	HWA3 [1)]	DI	Hardware address bit 3	-
27	HWA2 [1)]	DI	Hardware address bit 2	-
28	HWA1 [1)]	DI	Hardware address bit 1	-
29	HWA0 [1)]	DI	Hardware address bit 0	-
30	TRG	DI	Hardware trigger record measured value	
31	ZERO	DI	Counter reset/Load PRESET	
32	TEACH	DI	Teach: Set count value as PRESET	
33	NRES	DI	Reset, low active	10k → VDDO
34/35	VDD	DP	Power supply voltage digital	3.3 V
36/37	VSS	DP	Digital GND	GND
38	LDP	AO	Laser diode output positive	
39	LDN	AO	Laser diode output negative	
40	OPO	AI	Laser diode controller filter Out	
41	OPI	AI	Laser diode controller filter In	
42	VDDA	AP	Power supply voltage analogue	3.3 V
43	VSSA	AP	Analogue ground	GND
44	SMON	AIO	Analogue test input/Monitor sine channel	
45	CMON	AIO	Analogue test input/Monitor cosine channel	
46	V1P1	AO	Mean voltage instrumentation amplifier	(1.1 V)
47	VRH	AO	ADC reference voltage positive	(1.6)
48	ADIN	AI	Test ADC pin	
49	ADIP	AI	Test ADC pin	
50	VRM	AO	ADC reference voltage mean	(1.1 V)
51	VRL	AO	ADC reference voltage negative	(1.6)
52	VDDA	AP	Power supply voltage analogue	3.3 V
53	VSSA	AP	Analogue ground	GND
54	TSTP	AO	Analogue test output, configurable	
55	TSTP2	AO	Analogue test output, configurable	
56	TSTP1	AO	Analogue test output, configurable	
	EXPOSED			

AP = Power Supply Analogue, DP = Power Supply Digital, SP = Power Supply Sensor
AI = Input Analogue, AO = Output Analogue, AIO = Bidirectional Analogue
DI = Input Digital, DO = Output Digital
[1)] HWA0/1 → Gain 0/1
HWA2/3 → Low-pass filter enable

5.1 Package



	PACKAGE TYPE					
JEDEC OUTLINE	MO-220			MO-220		
PKG CODE	WQFN(X856)			VQFN(Y856)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.203 REF.			0.203 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30
D	8.00 BSC			8.00 BSC		
E	8.00 BSC			8.00 BSC		
e	0.50 BSC			0.50 BSC		
L	0.30	0.40	0.50	0.30	0.40	0.50
K	0.20	—	—	0.20	—	—

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
189X18* MIL	4.32	4.37	4.42	4.32	4.37	4.42	V	X	(W)VLLD-2
189X21* MIL	4.55	4.60	4.65	4.25	5.30	5.35	X	V	(W)VLLD-2
240X24* MIL	5.85	5.90	5.95	5.85	5.90	5.95	V	X	(W)VLLD-2

"*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

3RD ANGLE SYS.

比例 SCALE: | 材質 MTRL: | 製程 FINISH: | 數量 Q'TY:

圖名: THERMALLY ENHANCED PLASTIC VERY THIN AND VERY VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE QFN 56 TERMINALS (8.0X8.0mm)X856/Y856

圖號: J1-10056-002

圖檔: J1-10056-002-04 | 版次: 04 | 張數: 1/1

Figure 3: AM-IP4k QFN56 Package Dimensions

6 Startup behaviour / Configuration options

6.1 Reset

After the IC's reset the digital interface will be selected (SPI or SSI) and all registers will be initialised with their default values. In case a valid identifier was programmed at EEPROM address 0x00, the configuration values are read in from the internal EEPROM.

During the whole reset sequence one of the outputs `MISO` or `NERR` is maintained at L-level depending on the selected interface. Until this point the serial interfaces must not be activated. After completed initialisation the IC's configuration could be modified via the serial interface SPI[1]. The following tables show all required configurations to be determined by the user while resetting.

Table 2: Clock generator selection (Pin CLK_CLKSEL)

Signal at Pin CLK_CLKSEL	Clock generator	Frequency
GND	Internal oscillator	40 MHz
Clock	External clock at CLK_CLKSEL	max. 40 MHz

Table 3: Serial interface selection AM-IP4k

Interface	SEN reset value	Pin MISO / SLO	Pin MOSI / SLI	Pin SCK	Pin SEN	Ready signal
SPI	1	SPI-MISO	SPI-MOSI	SPI-SCK	SPI-SEN	at MISO
SSI	0	SSI-DATA	-	SSI-MA	0	at NERR

Table 4: Switching of configuration source

Content of EEPROM address 0x00	Configuration
Unequal 0x134A	Basic configuration → see tables 6, 7
0x134A	Read from EEPROM

6.2 Configuration

The IC can be adapted to various measuring systems and consecutive electronic systems by configuration registers. All setting options will be available if the IC is initialized using the EEPROM or serial interface (SPI). Table 5 gives an overview of the adjustment options of the AM-IP4k. Tables 6 and 7 provide its factory settings.

Table 5: Configuration options

Parameter	Possible values	Register / Bit
Interpolation rate	4096, 4000, 3200, 2048, 2000, 1600, 1024, 1000, 800, 512, 500, 400, 256, (250), 200, 128, (125), 100, 64, (50), 32, (25), 16, 8, 4, individual values[2]	CFG1 / IR(4:0) CFG2 / IRDIV2(1:0)
Minimum edge separation t_{pp}	1, 2, 4, 8, 16, 32, 64, 128	CFG1 / TPP(2:0)
Reference signal processing	Enable, disable, delayed Index 1 period / 1 increment Position 0°-360°, step size IRATE/360° Mode reset, trigger, adjust, distance coded	CFG3 / DISZ, ZDEL2 CFG3 / Z4 CFG4 / ZPOS2 CFG3 / ZMODE
Signal amplitude nominal	1000, 500, 250, 75 mV	CFG1 / GAIN(1:0)
Analogue low-pass filter	10 kHz, 75 kHz, 250 kHz, inactive	CFG2 / LP(1:0)
Digital hysteresis	0 (Disable), 1 … 7 (on/off)	CFG1 / DH(2:0)
Output signals A/B/Z	ABZ, DSP mode, sensor and reference point adjustment	CFG1 / MODE(2:0)
Error processing	Masking, latch enable Behaviour of ABZ outputs in case of error	CFG1 / Mxxx, Lxxx CFG1 / HLD, TRI

1 Only with an active SPI, not at SSI mode.
2 At EEPROM a table with specific interpolation rates can be stored. If the correction function is used, a corresponding correction table must be stored at EEPROM too.

Parameter	Possible values	Register / Bit
Phase correction	± 10° Step size 0.3125°, ±5° Step size 0.15625°	CFG2 / PHBER, PH(2:0) CFG3 / PHRENA
Gain controller	Default setting / time constant / enable, disable	CNTRLG, CFG2 / GAINCTL, DISCTL
Offset controller	Default setting / time constant / enable, disable	CNTRLO, CFG2 / OFFSCTL, DISCTL
Hardware address	0-15	CMD / SETHWA
Special functions	Trigger edge Teach active / inactive Measuring timer Counter zero position (preset)	CFG2 / TRGSLP CFG2 / TEAEN CFG3 / VT(1:0),T(7:0) PRE_ST, PRE_MT
Interface configuration	Data format of position values SPI mode synchronous, asynchronous SSI timing	CFGSSI / SSI20, MTBIT (1:0), GRAY, STBIT (4:0) CFG2 / ASYNC, SYNC(6:0) CFGSSI / SSITO, RING

Detailed descriptions of all the configuration bits can be found in chapter 9.

Table 6: Default settings

Configuration	Default (EEPROM with factory settings)		Default (Invalid EEPROM)	
Analogue	Phase correction Low-pass -1dB Nominal amplitude	0° Disabled 1000 mVpp	Phase correction Low-pass -1dB Nominal amplitude	0° Disabled 1000 mVpp
Interpolation	Interpolation rate Controller Controller start values Reference point	4096 Active, slow Mean value At 45°	Interpolation rate Controller Controller start values Reference point	4000 Active, slow Mean value At 0°
ABZ outputs	Mode TPP Digital Hysteresis Z Output in case of error	ABZ 0 1 Active, 1 increment Hold	Mode TPP Digital Hysteresis Z Output in case of error	ABZ 0 1 Active, 1 increment Hold
Error processing	Error monitoring Error storage	All errors (ABZ mode) Active	Error monitoring Error storage	All errors (ABZ mode) Inactive
Special functions	Teach Preset values	Active via `CFG2/TEAEN` 0x00	Teach Preset values	Inactive 0x00

Table 7: Default interface settings

Configuration	Default (EEPROM with factory settings)		Default (Invalid EEPROM)	
SPI interface	Activate via pin `SEN` **Hardware address at `HWA`**		Activate via pin `SEN` **Hardware address 0000**	
SSI interface	Activate via pin `SEN`		Activate via pin `SEN`	
	Timeout mode Format	20 µs @ 40 MHz, ring 13 bit single-turn	Timeout mode Format	20 µs @ 40 MHz, ring 13 bit single-turn

7 Functional description

7.1 Input amplifier / Low-pass filter

The AM-IP4k contains three instrumentation amplifiers with adjustable gain factors. Incremental encoders with a voltage interface and measuring bridges can be connected directly. Sensors with current interface are adapted by a simple external circuit (see chapter 11.1). The IC is able to operate with both single-ended and differential input signals. There is an identical amplification of all sensor signals (sine, cosine, reference). The mean voltage of the instrumentation amplifier at pin `V1P1` can be used to adapt the AM-IP4k to customised sensors. The instrumentation amplifiers are connected to the internal A/D converters either directly or via a configurable low-pass filter (see table 9). The voltage level at the A/D converter inputs can be monitored using the pins `SMON` and `CMON`.

Table 8: Nominal amplitude configuration (Register `CFG1`)

CFG1/GAIN(1:0)	00	01	10	11
Input voltage for differential supply per input (mV_{pp}) [1]	500	250	125	37.5
Input voltage for single-ended supply (mV_{pp}) [2]	1000	500	250	75
Nominal input voltage $V_{DIFFNOM}$ (mV_{pp})	1000	500	250	75
Interpolation input voltage range V_{DIFF} (mV_{pp})	600...1200	300...600	150...300	45...90
Mean voltage at input	2.5	2.5	2.5	2.5
Nominal output voltage V_{MON} at `SMON` / `CMON` (V_{pp}) [WIDE = 0]	0.635	0.635	0.635	0.635
Nominal output voltage V_{MON} at `SMON` / `CMON` (V_{pp}) [WIDE = 1]	1.27	1.27	1.27	1.27
Nominal mean voltage at `SMON` / `CMON`	1.1	1.1	1.1	1.1
Gain factor ($2xV_{MON} / V_{DIFF}$)[3]	1.27	2.54	5.24	16.76

[1] at each of the inputs `SINP`, `SINN`, `COSP`, `COSN`
[2] `SE_amp2` = 1, `SE_HALB` = 1
[3] WIDE = 0, `SE_AMP2` = 0, `SE_HALB` = 0

Table 9: Low-pass filter configuration (Register `CFG2`)

Cut-off frequency -1dB	CFG2/LP(1:0)
Low-pass filter inactive	00
250 kHz	01
75 kHz	10
10 kHz	11

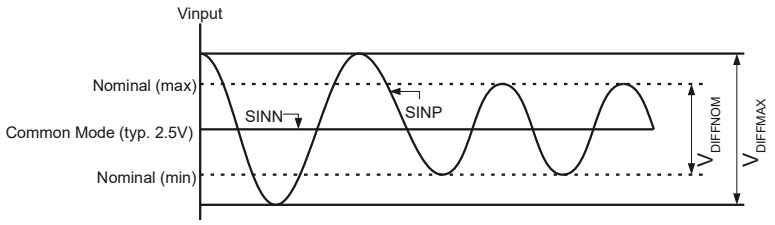


Figure 4: Input signals (single-ended)

While operating in single-ended mode the nominal signal amplitude has to be applied on the respective P-channel. The bits `SE_amp2` and `SE_halb` in register `CFG3` must be set to avoid the overriding of the differential input stage.

The mean voltage of 2.5 V has to be applied to the unused N-inputs. With bit `SE_VR_int` at Register `CFG3` activated, the mean voltage will be provided internally.

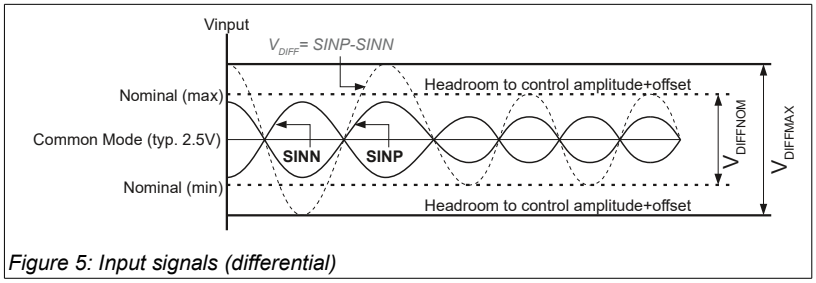


Figure 5: Input signals (differential)

The input voltage of the instrumentation amplifiers is limited within a range of V_{input}= 0.65 V to VDDA-0.45 V. Depending on the common-mode voltage at the analogue input, this may limit the operating range of the GAIN setting “00” (V_{NOM} = 1000 mV_{pp}), gain factor. Fehler: Referenz nicht gefunden

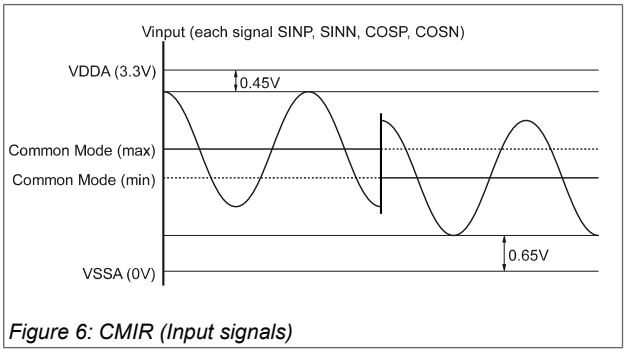


Figure 6: CMIR (Input signals)

The following table shows some combinations of common-mode voltage and supply voltage for single-ended signals[3] with a maximum amplitude of 1200 mV_{pp} and a maximum offset of ±100 mV:

Table 10: Example of common mode input voltage (CMIR)

VDDA	Common-mode voltage (Min)	Common-mode voltage (Max)
3.30 V	1.35 V	2.15 V
3.15 V	1.35 V	2.00 V
3.00 V	1.35 V	1.85 V

7.2 Signal adjustment

7.2.1 Amplitude and offset

The input signals are subjected to an AMAC-specific internal gain and offset control. The amplitudes are controlled within a range between 60 % and 120 % of the nominal amplitude. The control range of the offset of both input signals is ±10 % of the nominal amplitude.

After the IC’s reset, the start values are loaded from the EEPROM to correct input signals’ amplitude and offset. The IC will reach full measuring accuracy only after the transient oscillation of the internal signal control, which means after about 10 to 50 sine periods.

The phase potentiometer has to be matched with the sensor connected to the AM-IP4k for the highest possible accuracy of amplitude and offset control.

Amplitude and offset errors are considered as one unit. This means for some applications the decrease of one of the errors could possibly go along with an admissible increase of the other parameter’s error. The attenuation of the controlled system implemented in the AM-IP4k can be adjusted (registers `CFG2/GAINCTL` and `CFG2/OFFSCTL`).

During the process of adjustment, the input frequency must be only 50 percent of the specified maximum frequency.

3 with `SE_amp2` = `SE_halb` = 0

7.2.2 Phase Adjustment

The phase deviation of the input signal can be corrected statically or tuned via a 64 step digital potentiometer.

For a static phase adjustment the register bits `CFG2/PHBER` and `CFG2/PH` should be set accordingly. By configuring bit `CFG2/PHBER` two possible setting ranges can be selected[4]:

- ±5° Step size 0.15625°
- ± 10° Step size 0.3125°

In register bits `CFG2/PH` the calculated correction value (in signed format), from the following formula should be entered[4]:

$$PH = round\left(-\frac{Deviation[°]}{Stepsize[°]}\right) \quad [1]$$

If the automatic phase correction (phase controller) is used, then the configuration bit at `CFG3/PHRENA` should be activated. Then the phase adjustments at `CFG2/PHBER` and `CFG2/PH` are disregarded. And the phase correction value is now taken from the integrated phase controller.

7.3 Signal correction (Periodic errors)

Two corrections can be applied to the sampled signal for periodic error compensation. The 360° correction (wobble correction) of position errors during a complete sensor rotation is suitable only for rotary encoders. In contrast, the SC correction[5] (signal form correction) analyses a single sine period of the sensor signal and therefore can be applied to linear encoders, too.

The corrections can be activated and deactivated separately, but only work with a valid loaded EEPROM configuration. Besides general settings, this configuration has to contain the proper correction coefficients for a particular input signal.

Table 11: Register "Correction"

Name	SPI address [bit]	EEP address [bit]	Function
DISKSC	0x13 [2]	0x09 [10]	'1' = SC correction off
DISK360	0x13 [1]	0x09 [9]	'1' = 360° correction off
Koeffizienten_360	0x40...0x5F	0xA0...0xBF	Table of coefficients for 360° correction
Koeffizienten_SC	0x60...0x7F	0xC0...0xDF	Table of coefficients for SC correction
Zahnzahl	0x1B [4:0]...0x1A [7:0]	0x0D [12:0]	Number of teeth for 360° correction
KorrekturwertSC	0x94...0x97	-	Calculated correction value SC correction
Korrekturwert360	0x98...0x9B	-	Calculated correction value 360° correction
LDR_OUT	0x9C...0x9F	-	Output value of laser diode control

The flag `EKOVL` at the register `STAT/ID/RE` shows whether there is an error in the calculation of the correction. If this is the case and other errors are discarded, then the validity of the coefficients and of the number of teeth should be checked.

Both third order corrections are structured like this:

$$p_0 \cdot fs^3 + p_1 \cdot fs^2 \cdot fc + p_2 \cdot fs \cdot fc^2 + p_3 \cdot fc^3 + p_4 \cdot fs^2 + p_5 \cdot fs \cdot fc + p_6 \cdot fc^2 + p_7 \cdot fs + p_8 \cdot fc + p_9 \quad [2]$$

4 The reference signal for the phase deviation is SIN. A phase deviation is considered to be positive when the phase increases between the SIN and COS.

5 SC = Sin/Cos

The correction coefficients p are calculated using the measured sine and cosine signals and the phase deviation of the Levenberg–Marquardt algorithm including the least-squares method. An implementation based on Joachim Wuttke's version is used.[6]

The parameters of the function 'lmmin' are defined as follows:

```
 n_par:                  Number of coefficients (= 10 for third order)
par:                     Start parameter (First approximation, may be equal to {0}) or
              return of the calculated coefficients
m_dat:                   Length of the signal vector (sine/cosine)
data:                    Array with sine, cosine, Y_Soll[7] and structure of the correction
function kf
              (see equation above [2])
evaluate:     Parameter of an additional function for calculation
              (see the algorithm below)
control:      Fitting parameter (see table 12)
status:                  Status information for calculation
printout:     Internal function 'lm_printout_std'
```

The residuum's calculation is processed with the 'evaluate' function according to the following algorithm:

```
for i = 0 to m_dat-1
          fvec[i] = kf(Sin[i], Cos[i], par) - Y_Soll[i]
end
```

with

```
fvec:     Output array of length m with the current estimated value
```

Table 12: Control parameter of coefficient calculation

Name	Value	Description
control	lm_control_double	Calculating with double accuracy
control.ftol	5*DBL_EPSILON	Relative error desired in the sum of squares
control.xtol	5*DBL_EPSILON	Relative error between last two approximations
control.gtol	5*DBL_EPSILON	Orthogonality desired between fvec and its derivs
control.epsilon	5*DBL_EPSILON	Step used to calculate the jacobian
control.stepbound	1000	Initial bound to steps in the outer loop
control.maxcall	1000	Maximum number of iterations
control.scale_diag	1	Automatic diag rescaling
control.printflags	3	OR'ed to produce more noise
DBL_EPSILON is a constant for the accuracy of the arithmetic, depending on the system used for the calculation.		

The data format of the coefficients is signed and it is 16 or 18 bit, depending on the setting `MXSHR` at register `CFG3`.

6 http://apps.jcns.fz-juelich.de/doku/sc/lmfit
7 Y_Soll = Position error

7.4 Interpolation

The signal periods of the analogue input signals sine and cosine are divided according to the selected interpolation rate and transferred as a count value via the serial interfaces (SPI/SSI) to following components. Square-wave sequences with a 90° phase shift (A/B/Z signals) are generated in parallel. Furthermore the number of detected reference marks is counted with the correct sign. So for rotary encoder applications a so-called multi-turn counter is integrated into the IC.

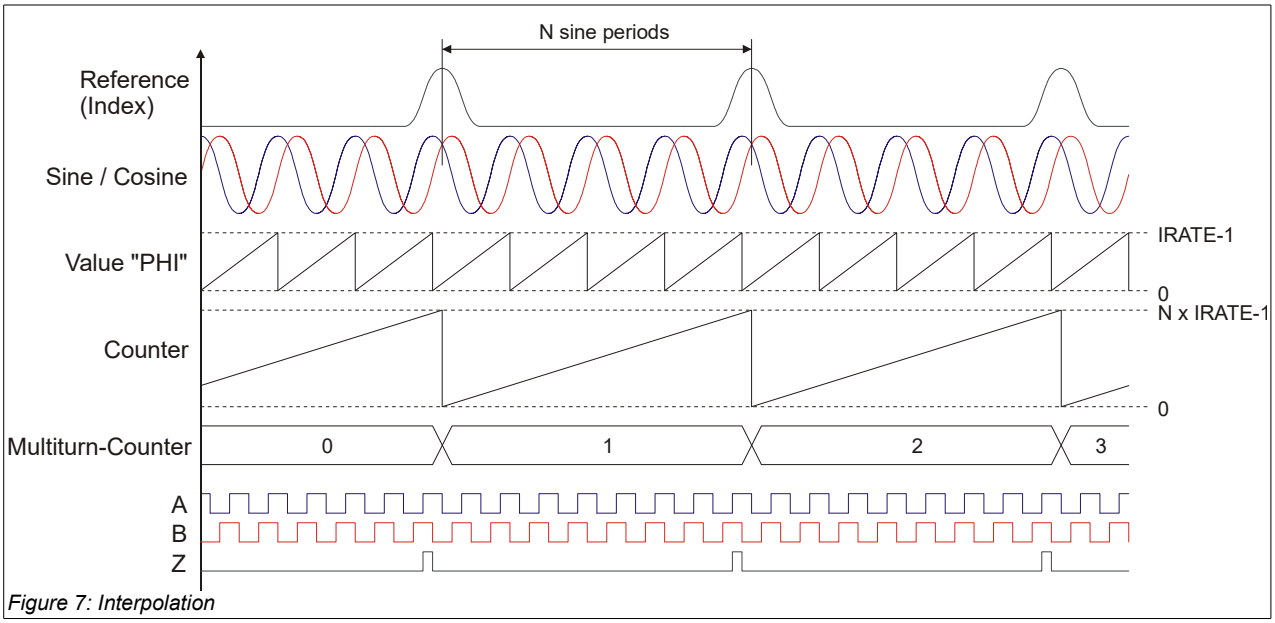


Figure 7: Interpolation

7.4.1 Interpolation rate

The interpolation rate (IRATE) can be selected from the given values in table 13. Interpolation rate in this context means the number of increments into which a sine or cosine input signal period can be divided. This corresponds to the number of signal transitions at the A/B outputs per input signal period. The number of square wave periods at the A/B outputs is a quarter of the interpolation rate.

The interpolation rate is configured at CFG1/IR. There are four basic interpolation rates: 4096, 4000, 3200, and 2560. The last has a factory setting value and can be reprogrammed by user. The succeeding interpolation rate values correspond to the division by 2, 4, 8, 16, 32, 64, and 128 of basic interpolation rates. Invalid values occur when result division is not an integer.

Table 13: Interpolation rate

IR(2:0) / IR(4:3)	000	001	010	011	100	101	110	111
10	**4096**	2048	1024	512	256	128	64	32
00	**4000**	2000	1000	500	250[1)]	125[1)]	Invalid	Invalid
01	**3200**	1600	800	400	200	100	50[1)]	25[1)]
11[2)]	**2560**[3)]	1280	640	320	160	80	40	20

[1)] Interpolation rates may be used only in the counter mode. ABZ signals are invalid.
[2)] Address for interpolation rates to be chosen freely (EEPROM).
[3)] Factory setting for basic interpolation rate, which can be chosen freely.

It is also possible to select further interpolation rate values with an extended IR divider. The basic interpolation rates remain the same. Using configuration IRDiv2 in CFG2 the interpolation rates 16, 8, and 4 can be selected. See Table 14.

IR_sum(3:0) = IR(2:0) + IRDiv2(2:0)

Table 14: Interpolation rate with extended IR divider

IR_sum / IR(4:3)	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010
10	**4096**	2048	1024	512	256	128	64	32	16	8	4
00	**4000**	2000	1000	500	250[1)]	125[1)]	Invalid	Invalid	Invalid	Invalid	Invalid
01	**3200**	1600	800	400	200	100	50[1)]	25[1)]	Invalid	Invalid	Invalid
11	**2560**	1280	640	320	160	80	40	20	Invalid	Invalid	Invalid

[1)] Interpolation rates may be used only in the counter mode. ABZ signals are invalid.

7.4.2 Edge separation control / Interval time t_{pp} / Hysteresis

The output signals A, B, and Z vary with a time gap t_{pp}, which can be limited to a minimum by the configuration bits CFG1/TPP(2:0). The time interval depends on the oscillator frequency and can be set in binary steps. After switching one of the outputs the other signal's consecutive edge will only be visible at the IC's output after time t_{pp} has elapsed. Thus a connected interpolation counter will operate accurately even when a short-time disturbance of the input signals occurs. The interval time can be set by the IC's user according to the counter connected to the outputs A, B, and Z (see chapter 7.5). This causes a step size at the IC's output varied in time which has to be taken into consideration.

The AM-IP4k uses a digital interpolation method resulting in an interference of the speed-proportional output signals by inevitable quantification errors (the so-called ±1 errors). These errors can be suppressed by activating the digital hysteresis (Register CFG1/DH) so switching of the outputs in case of static input signals will be prevented. In doing so, all output signals will be delayed for the set hysteresis value.

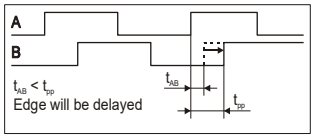
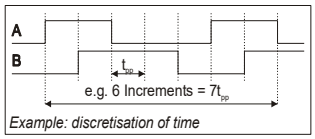
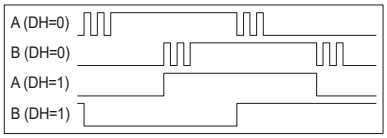


Figure 8: Edge separation control



Time discretisation



Hysteresis

7.4.3 Index signal Z

The index signal Z will be generated if the differential voltage between the reference inputs REFP and REFN is positive and also if the analogue sine and cosine signals have the phase angle defined at register CFG4 using the bits ZPOS2(15:0). This phase angle is set to 0° by default. The width of the index signal Z can be modified between 1 and 4 increments at the IC's output, which means between ¼ and 1 period of the output signals A and B(CFG3/Z4). If the IC is set to the index width of 1 increment (¼ period), the outputs A and B will have a H-level with the Z-signal activated.

The phase angle adjustment to detect a sensor's reference signal could be done using test signals or a trigger mode, see chapter 7.8.

The figure below shows the relation between the analogue input signals, the output signals A, B, and Z plus the integrated counter's value.

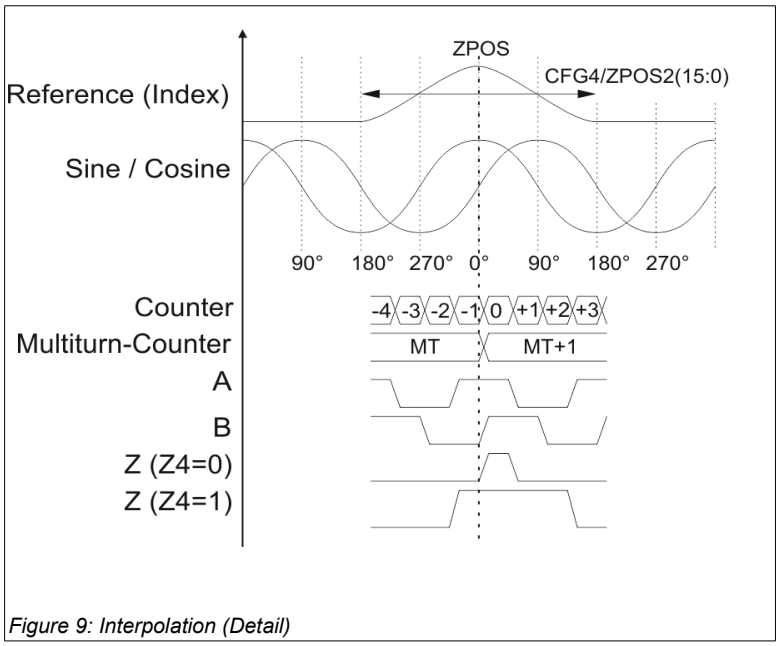


Figure 9: Interpolation (Detail)

7.5 Mode / Maximum input frequency

The maximum input frequency depends on the selected interface at the output. If square-wave signals (A/B/Z) are used as output signals, the maximum input frequency will be limited by the interpolation rate and the minimum edge separation (t_{pp}).

And when only the internal count value is processed (SPI or SSI interfaces), then the maximum input frequency will be determined by the IC's clock frequency (f_{OSZ}).

The mode is switched by the bit MABZ at the register CFG1. Only at square wave ABZ mode is possible to enable the monitor frequency error detection. If both output interfaces are meant to be used simultaneously the bit MABZ must be initialised with "1".

Table 15: Maximum input frequency

Mode	CFG1/MABZ	Maximum frequency for the counter	Maximum frequency for the ABZ output
Counter	0	$f_{max} \approx f_{OSZ} / 180$	No error detection
Square wave, $t_{pp} = N/f_{OSZ}$ $N = 2^{CFG1\text{-}TPP(2:0)}$	1	$f_{max} \approx 0.9 \cdot f_{OSZ} / IRATE < f_{OSZ} / 180$	$f_{max} \approx 0.90 \cdot f_{OSZ} / (N \cdot IRATE) < f_{OSZ} / 180$ (if N=1) $f_{max} \approx 0.95 \cdot f_{OSZ} / (N \cdot IRATE) < f_{OSZ} / 180$ (if N>1)

The maximum limit of the input frequency is about 220 kHz, with a IC's clock frequency of f_{OSZ} = 40 MHz, and a guaranteed edge separation t_{pp} of 32 µs maximum with a clock frequency of 4 MHz. The AM-IP4k can be adapted to the consecutive electronics by varying the clock frequency and the edge separation appropriately between these two values. All values apply to a phase adjusted between the input signals and after the transient oscillation, of the internal signal control. Up to this point the input frequency has to be only 50 % of the specified maximum frequency.

ⓘ *As the maximum input frequency is exceeded the relevant error bit is set (chapter 7.6).*

ⓘ *The configuration of the analogue low-pass filter also limits the maximum input frequency. See chapter 7.1 for details.*

7.6 Sensor monitoring

The AM-IP4k provides up to 7 possibilities to monitor the sensor signals and to detect errors at the analogue input signals. Each monitoring source can be activated, deactivated, or be configured by the respective bits at the register CFG1 or with memory behaviour. If the respective monitoring flags are enabled, the detected or saved error signals will be output at pin NERR. The monitoring flags can be read via the serial SPI interface. Summarised information of any error or warning is available via the SSI interface.
In general, the behaviour of the outputs A, B, and Z will be not defined if an error occurs. If the bit HLD is set at register CFG1, the outputs will not change in case of an error. If the bit TRI is set at register CFG1, the outputs A, B, and Z will get a high-impedance state in case of an error. A consecutive evaluation unit is able to identify this kind of state as an error mode.

ⓘ With an activated error signal NERR or with one of the monitoring flags set at the result register, the current measurement result and all subsequent results must be discarded. After the removal of the cause of error and the resetting of the error bits using the SPI command RESCNT or the ZERO signal, it is necessary to cross the reference point again to be able to measure absolute values.

Table 16: Sensor monitoring overview

	Name	Meaning	SPI	ABZ	SSI
1	EVLOW	The signal vector, generated by sine and cosine signal, is to small.	Status bit	Error	Error
2	ESADC / ECADC	One or both A/D converters are over-driven.	Status bit	Error	Error
3	ESOFF / ECOFF	The offset controller has reached its limit.	Status bit	Error	Warning
4	ESGAIN / ECGAIN	The gain controller has reached its limit.	Status bit	Error	Warning
5	EFAST	The input frequency is too high.	Status bit	Error	Error
6	EKOVL	The calculated correction value is invalid.	Status bit	Error	-
7	EABZ	The signals A, B, and Z are invalid.	Status bit	Error	-

The recommended configuration of the sensor monitoring depends on the selected interfaces. The configuration is done, by the user, setting the relevant bits at register CFG1. The general recommendation is to activate all monitoring sources. It will be possible to deactivate the monitoring of the maximum ABZ frequency (bit MABZ) if the IC operates counter mode (without the outputs A, B, and Z), see chapter 7.5.

Table 17: Recommended configuration for sensor monitoring

	ABZ interface	SPI interface	SSI interface
Activated monitoring bits	EVLOW EADC EOFFS EGAIN EFAST EKOVL[1)] EABZ	EVLOW EADC EOFFS EGAIN EFAST EKOVL[1)]	EVLOW EADC EOFFS EGAIN EFAST EKOVL[1)]
Processing of the monitoring bits	As total error in the error signal at pin NERR	Status register Position register Error signal NERR	As 2 bit total error and -warning in data stream.
Enable storage of the monitoring bits	Deactivate	Activate	Activate
Clearing of the error memory	-	Command RESCNT ZERO signal	ZERO signal
ABZ behaviour in case of error	Hold and/or tristate	Any behaviour	Any behaviour
Register CFG1(31:16)	0x007F	0x3777	0x3777

[1)] with activated corrections

7.6.1 Sources of error

The monitored sensor signal parameters are described in detail below. For each monitoring source the corresponding bits at the registers CFG1 and STAT are given.

Vector error

The signal vector generated from the sine and cosine signal is smaller than appropriately 30% of the nominal amplitude, caused mostly by a partially or totally disconnected sensor. Another cause of error are input signals with a very large offset and a low amplitude at the same time.

Activation of error detection	Activation of error storage	Register STAT	SSI DATA
Bit MVLOW	Bit LVLOW	Bit EVLOW	Bit0 – Error (H-active)

ADC error

One or both A/D converters are over-driven, caused by a signal amplitude being too high. Input signals with a very large offset and a low amplitude at the same time are another source of error. If there are suitable pull-up and pull-down resistors at the sensor inputs, partially or totally disconnected sensors can be detected by this error bit too.

Activation of error detection	Activation of error storage	Register STAT	SSI DATA
Bit MADC	Bit LADC	Bit ESADC (Sine) Bit ECADC (Cosine)	Bit0 – Error (H-active)

Offset error

The offset controller has reached its limit, caused by a signal offset being too large, a partially or totally disconnected sensor, or an invalid value for the initialisation of the offset controller.

Activation of error detection	Activation of error storage	Register STAT	SSI DATA
Bit MOFF	Bit LOFF	Bit ESOFF (Sine) Bit ECOFF (Cosine)	Bit1 – Warning (H-active)

Amplification error

The gain controller has reached its limit, caused either by a signal amplitude being too low, or by a partially or totally disconnected sensor.

Activation of error detection	Activation of error storage	Register STAT	SSI DATA
Bit MGAIN	Bit LGAIN	Bit ESGAIN (Sine) Bit ECGAIN (Cosine)	Bit1 – Warning (H-active)

Speed error

The input frequency is too high to generate A/B signals or to detect the direction. The monitored frequency differs in the use of the internal counter and the square-wave outputs A/B/Z, see chapter 7.5.

Activation of error detection	Activation of error storage	Register STAT	SSI DATA
Bit MFAST	Bit LFAST	Bit EFAST	Bit0 – Error (H-active)

Correction error

An error occurred while calculating the correction values. A wrong configuration of the correction coefficients and/or the number of teeth causes these invalid correction values.[8] The sensor should be calibrated again, see chapter 7.7.4

Activation of error detection	Activation of error storage	Register STAT	SSI DATA
Bit MKOVL	Bit LKOVL	Bit EKOVL	-

ABZ error

The signals A, B, and Z are invalid because of the input frequency being to high. The monitored frequency depends on the defined minimum edge separation t_{pp}. This error bit will be also set if the interpolation rate or the minimum edge separation t_{pp} are changed. If the AM-IP4k is used with the internal counter only, the detection of

8 The number of teeth is only needed for 360° correction and is equivalent to the number of sine/cosine periods during a single 360° turn.

this error must be deactivated (MABZ = 0).

Activation of error detection	Activation of error storage	Register STAT	SSI DATA
Bit MABZ	Bit LABZ	Bit EABZ	Bit0 – Error (H-active)

7.7 Outputs ABZ

The meaning of the signals at the outputs A, B, and Z can be modified using the bits MODE at register CFG1. The standard square-wave sequences with an offset of 90°, are generated by default. If the IC's internal counter is used, the "Controller/DSP" mode can be activated. Thus it is possible to perform equidistant measurements, to synchronise additional components with the IC or to transfer measured values in an interrupt-controlled way to a processing IC. In three other modes test signals are provided at the outputs A, B, and Z for sensor adjustment.

Table 18: ABZ modes (Register CFG1)

Mode	Use/ Meaning	CFG1/MODE	Output A	Output B	Output Z
Standard	Standard ABZ	000	Square-wave sequence A	Square-wave sequence B	Index signal Z
Sensor adjustment 1	Sensor adjustment	001	Test signal IR4C	Test signal IR4S	Reference comparator REFCOMP
Sensor adjustment 2	Sensor adjustment	010	Test signal IR8C	Test signal IR16C	Control deviation NDEV
Sensor adjustment Z	Reference position adjustment	011	Reference (synchronous) REF_SYNC	Counter index point ZCNT	Index signal Z
MC/DSP	Counter to microcontroller	100	Timer-/Trigger-Interrupt nINT	Synchronising signal StartSample	Counter index point ZCNT
Calibration mode for correction	Calculation of the correction coefficients	111	Square-wave sequence A	Square-wave sequence B	Index signal Z

7.7.1 Standard ABZ

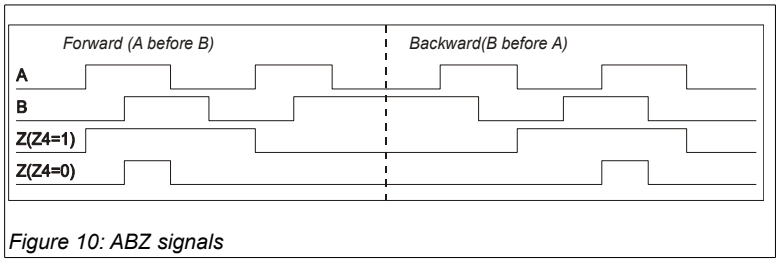


Figure 10: ABZ signals

7.7.2 Controller / DSP

Additional signals will be provided at the outputs A, B, and Z if the measured values are transferred via serial interface (SPI/SSI) exclusively. The output NERR keeps its meaning. It is designed as an open drain pin so as to connect the error signals of several ICs.

Table 19: DSP mode

Pin	Signal	Meaning
A	nINT	Interrupt; L-active; an active signal indicates at least one of the trigger holding registers is being occupied. A read-access to the register MVAL provides the “oldest” value saved at the registers. The interrupt can be triggered by the timer, the reference signal, or a signal at the input TRG. See chapter 7.8
B	StartSample	Synchronising signal; this signal provides the sampling time of the integrated A/D converters and can be used to synchronise other systems
Z	ZCNT	Counter index point; this signal indicates the AM-IP4k’s internal counter being reset at the reference point

7.7.3 Reference position adjustment

The phase angle for the detection of the reference signal can be shifted sensor-specifically by the configuration bits CFG4/ZPOS2 (see figure 9). For this purpose, specific auxiliary signals can be measured at A, B, and Z. The measured value trigger can be used additionally for reference position adjustment by initialising the configuration bits CFG3/ZMODE with the value “01”. The values TRGVAL1 and TRGVAL2 can be determined exactly by the read-out of the register MVAL (see figure 11). Referring to the interpolation rate this results in the reference signal width as well as the position of the processed index signal compared to analogue reference signal and to the sine sensor signal.

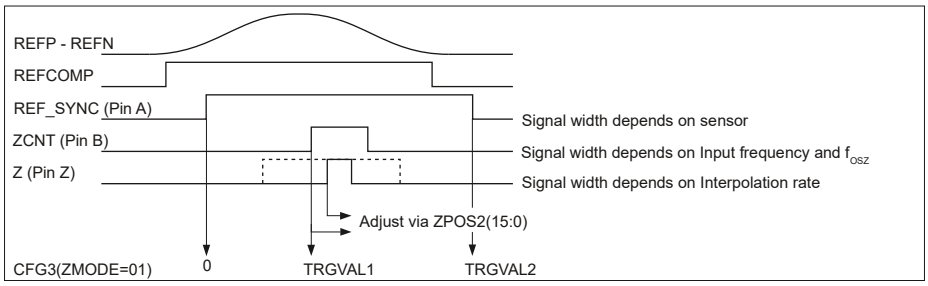


Figure 11: Reference signal adjustment

Reference signal width: Zwidth = TRGVAL2/IRATE·360°
Reference signal position: Zstart = ZPOS2/IRATE·360° - TRGVAL1/IRATE·360°
Reference value: TRGVAL1 = TRGVAL2/2
New setting value: ZPOS_new = (Zstart + Zwidth/2)/IRATE·360°

ⓘ IRATE is the undivided basic interpolation rate. The software for the evaluation of TRGVAL1 and TRGVAL2 should be able to identify that there is no index signal at the output (Z), also in case of doubled index signals were values of TRGVAL1 or TRGVAL2 are implausible or switching between different values. It is recommended to run the reference point adjustment with a low signal frequency compared to the oscillator frequency.

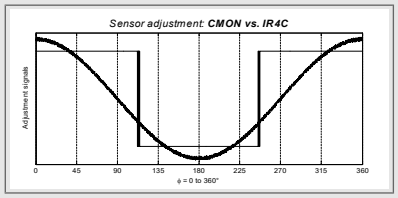
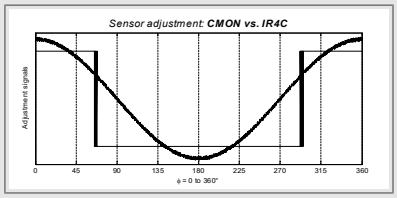
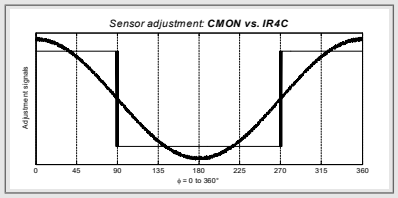
7.7.4 Sensor adjustment

The IC AM-IP4k automatically adjusts the offset and the amplitude of both encoder signals. It is useful to adjust static sensor errors previously to be able to use the full control range for dynamic errors. To this, in the modes “Sensor adjustment 1” and “Sensor adjustment 2”, auxiliary signals are provided for the fine adjustment of the sensor at the outputs A, B, and Z. The output signals of the instrumentation amplifiers can be measured at the outputs SMON and CMON. Table 20 gives a description of the adjustment procedure. Typical waveforms are shown in the following figures.

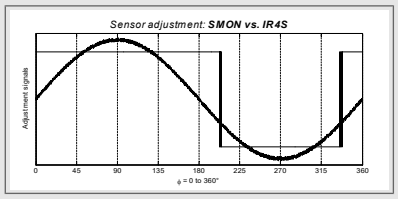
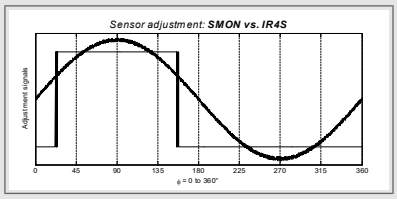
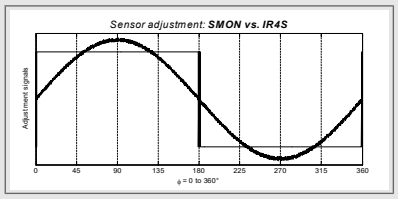
Table 20: Sensor adjustment

No.	Adjustment	Setting of the register	Instruction
1	Amplitude Sine/Cosine	Setting the gain factor CFG1/GAIN	Sensor movement. Measuring at the pins SMON and CMON. Adjustment until both amplitudes show approximately 1.27 Vpp.
2	Reference	Mode “Sensor adjustment 1”	Measuring of the signal REFCOMP. Adjustment until the signal width corresponds approximately one period of the sine signal.
3	Offset Cosine	Mode “Sensor adjustment 1” Deactivate controller (CFG2/DISCTL = 1). Correction values in the setting range’s middle.	Sensor movement. Measuring at CMON and signal IR4C. Adjustment until the duty cycle at IR4C is 50 % of the period at CMON.
4	Offset Sine	Mode “Sensor adjustment 1” Deactivate controller (CFG2/DISCTL = 1). Correction values in the setting range’s middle.	Sensor movement. Measuring at SMON and signal IR4S. Adjustment until the duty cycle at IR4C is 50 % of the period at CMON.
5	Phase (coarse)	Mode “Sensor adjustment 2” Activate controller (CFG2/DISCTL = 0).	Sensor movement. Measuring at CMON and signal IR16C. Coarse phase adjustment until all edges at IR16C are evenly spread within a sine period.
6	Phase (fine)	Mode “Sensor adjustment 2” Activate controller (CFG2/DISCTL = 0).	Sensor movement. Measuring at CMON and signal NDEV. Phase adjustment until frequency at NDEV does not correlate with the frequency of the sine signal.
7	Amplitude parity	Mode: “Sensor adjustment Z” Deactivate controller (CFG2/DISCTL = 1). Correction values in the setting range’s middle.	Sensor movement. Measuring at CMON and signal IR8C. Adjustment of the signal amplitudes until all edges at IR8C are evenly spread within the sine period.

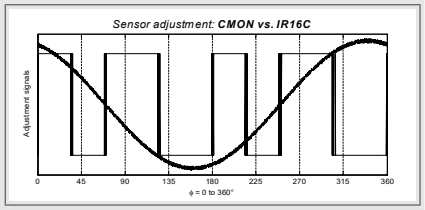
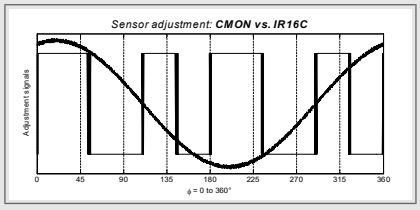
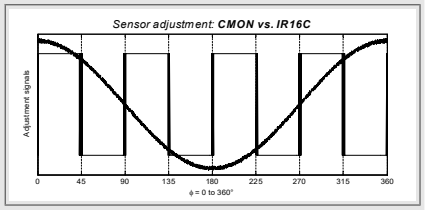
Adjustment offset cosine – Signals CMON and IR4C (Output A)
Mode '001' (Sensor adjustment 1), controller inactive / correction values: Mean value of the setting range

Offset cosine **positive**	Offset cosine **negative**	Offset cosine **adjusted**
Duty cycle IR4C > 50 %	Duty cycle IR4C < 50 %	Duty cycle IR4C = 50 %
		

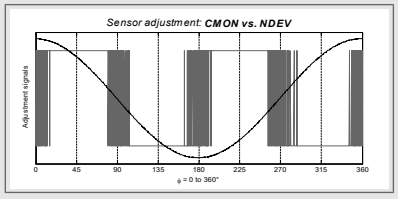
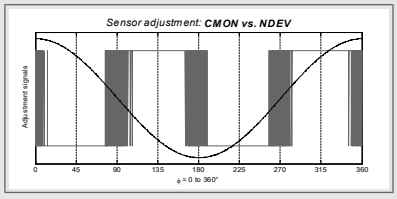
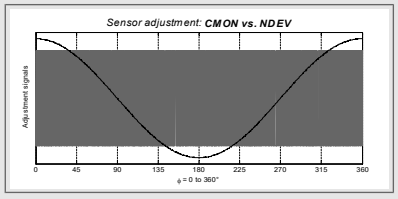
Adjustment offset sine – Signals SMON and IR4S (Output B)
Mode '001' (Sensor adjustment 1), controller inactive / correction values: Mean value of the setting range

Offset sine **positive**	Offset sine **negative**	Offset sine **adjusted**
Duty cycle IR4S > 50 %	Duty cycle IR4S < 50 %	Duty cycle IR4S = 50 %
		

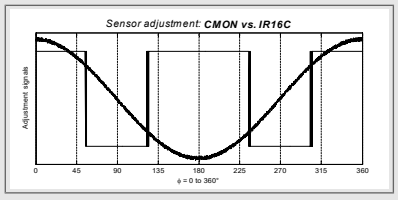
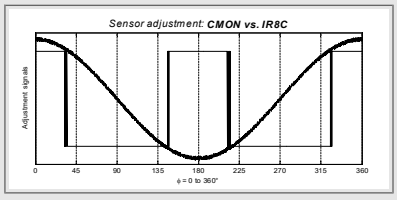
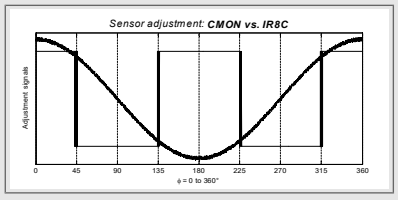
Adjustment phase (coarse) – Signals CMON and IR16C (Output B)
Mode '010' (Sensor adjustment 2), controller active

Phase between cosine and sine **> 90°**	Phase between cosine and sine **< 90°**	Phase between cosine and sine **adjusted**
Duty cycle IR16C ≠ 50 % H-L-edge IR16C at φ < 45°	Duty cycle IR16C ≠ 50 % H-L-edge IR16C at φ > 45°	Duty cycle IR16C = 50 % H-L-edge IR16C at φ = 45°
		

Adjustment phase (fine) – Signals CMON and NDEV (Output Z)
Mode '010' (Sensor adjustment 2), controller active

Phase between cosine and sine **>≈ 90°**	Phase between cosine and sine **<≈ 90°**	Phase between cosine and sine **adjusted**
Frequency(NDEV) ≈ ½·Frequency(CMON) H-level NDEV at φ = 45°	Frequency(NDEV) ≈ ½·Frequency(CMON) L-level NDEV at φ = 45°	Frequency(NDEV) >> Frequency(CMON)
		

Adjustment amplitude parity – Signals CMON and IRC8 (Output A)
Mode '010' (Sensor adjustment 2), controller inactive / correction values: Mean value of the setting range

Ampl. cosine **higher than** ampl. sine	Ampl. cosine **smaller than** ampl. sine	Ampl. cosine and ampl. sine are **equal**
Duty cycle IR8C > 50 %	Duty cycle IR8C < 50 %	Duty cycle IR8C = 50 %
		

7.8 Measured value trigger

The IC AM-IP4k has two trigger holding registers. The actual count value can be transmitted, when commanded by the hardware. The respectively “oldest” value is provided from the trigger holding registers when there is a read-access to the register MVAL. If no value is saved, the current count will be shown. The trigger holding register is enabled after being read out. The next to be read value’s trigger source is saved to the status register STAT. Furthermore the bit TRGOVL indicates whether a trigger pulse was lost, because of both trigger registers being occupied at the time the trigger pulse occurred. By the use of the bit TRG at the register MVAL it is possible to identify whether the read value was generated by a hardware event. The signal nINT at the output A indicates via the L-level whether one of the trigger holding register is occupied, see for details chapter 7.7.2.

Table 21: Trigger mode/Reference point modes

Trigger source	Use
TRG input	Trigger in case of events of external components (e.g. measuring probe). Trigger by microcontroller for equidistant measurements.
Timer	Trigger for equidistant measurements.
Reference CFG3/ZMODE=“01“	Trigger by reference/index signal for analysis with software.
Reference CFG3/ZMODE=“10“	Trigger by reference/index signal for adjustment of reference point position with software.
Reference CFG3/ZMODE=“11“	Trigger by reference/index signal for analysis of distance coded reference marks.

TRG input

The actual count value is written to one of the two trigger holding registers using a signal edge at input TRG. The active trigger edge is set by CFG2/TRGSLP.

Timer

After expiry of the internal timer, the actual count value is written to one of the two trigger holding registers. The timer’s time constant is set between $2^6/f_{osz}$ and $2^{16}/f_{osz}$ by the bits CFG3/VT and CFG3/T.

Reference trigger

Any occurrence of an index impulse leads to the transfer of the actual count value to one of the two trigger holding registers.

Adjustment of the reference position

The rising edge at the analogue reference signal resets the internal counter. The reference point detection by the IC at the set phase angle triggers the count value’s transfer to the first trigger holding register. The falling edge at the analogue reference signal causes the count value’s transfer to the second trigger holding register. After these two trigger events the bit ZSTAT is set and the trigger processing remains locked until the release by one of the SPI commands RESCNT or CLRZ. See also figure 11 and chapter 7.7.3.

Processing of distance coded reference marks

The first reference mark resets the internal counter, the second one triggers the transfer of the count value to a trigger holding register. After these two events the bit ZSTAT is set and the trigger processing remains locked until the release by one of the SPI commands RESCNT or CLRZ. The two reference marks have to differ by at least two input signal periods.

7.9 Registers of measured values

The interpolated count values, the trigger holding values, the position values, and the sensor monitoring information can be read out from several registers via the serial interface SPI. The following table gives an overview of which register to use for different applications and interfaces.

Table 22: Position registers

	SPI	SSI
Register CNT	Interpolation counter 30 bit Index status 1 bit Error status 1 bit	-
Register MVAL	Interpolation counter 30 bit or Trigger value 30 bit Trigger status 1 bit Error status 1 bit	-
Register POSIT	Interpolation counter 8-30 bit Multi-turn counter 0-16 bit Error status 2 bit	-
Register STAT	Error status 9 bit Trigger status 4 bit Index status 1 bit	-
SSI data	-	Interpolation counter 8-30 bit Multi-turn counter 0-16 bit Error status 2 bit

The data format of the position data (register `POSIT`) and of the SSI data is determined at register `CFGSSI` with the bits `STBIT`, `MTBIT`, and `GRAY`. The resolution of the multi-turn counter is selected between 0, 8, 12, and 16 bit by the bits `MTBIT`. The remaining bits of the transferred `POSIT` register are filled with bits of the single-turn counter. The configuration bits `STBIT` define how many bits (LSB) are valid within the single-turn counter; invalid MSB are filled with “0”. The coding of both count values can be switched between gray and binary code using the bit `GRAY`. In addition, the total length of the SSI data depends on the bit `SSI20`.

Table 23: Configuration of data format for positioning data

MTBIT	SSI20	Position data SPI Register `POSIT`	Position data SSI
00	0	30 bit single-turn / 8-30 bit resolution 1 bit error / 1 bit warning	30 bit single-turn / 8-30 bit resolution 1 bit error / 1 bit warning
01	0	8 bit multi-turn 22 bit single-turn / 8-22 bit resolution 1 bit error / 1 bit warning	8 bit multi-turn 22 bit single-turn / 8-22 bit resolution 1 bit error / 1 bit warning
10	0	12 bit multi-turn 18 bit single-turn / 8-18 bit resolution 1 bit error / 1 bit warning	12 bit multi-turn 18 bit single-turn / 8-18 bit resolution 1 bit error / 1 bit warning
11	0	16 bit multi-turn 14 bit single-turn / 8-14 bit resolution 1 bit error / 1 bit warning	16 bit multi-turn 14 bit single-turn / 8-14 bit resolution 1 bit error / 1 bit warning
XX	1	30 bit single-turn / 8-30 bit resolution 1 bit error / 1 bit warning	18 bit single-turn / 8-18 bit resolution 1 bit error / 1 bit warning

7.10 Counter preset / SPI commands / Control signals

The values of the integrated counter and of the integrated multi-turn counter can be preset. For this purpose the AM-IP4k contains some registers to hold the values to be set. In this way, an application-specific zero position can be configured independently of reference marks. This zero position can be stored permanently in conjunction with the integrated EEPROM. In addition, SPI commands and signals are implemented to read and store the configuration, as well as to command the controller and to set the counter.

Table 24: Commands/Control signals

Action	Counter and Reg. PRE_ST	Multi-turn counter and Reg. PRE_MT	Controller	EEPROM
Reference signal (at REFP/REFN)	Counter reset to 0	Counter: Incrementing or decrementing	-	-
Reset / SPI command RESIC [1]	PRESET register is loaded from the EEPROM, then this value is transferred to counter		Controller values are loaded from the EEPROM	Configuration is read out the EEPROM and written to the register
Reset / SPI command RESIC [2]	Counter reset to 0; PRESET register is initialised with 0		Reset to centre position	-
SPI command RESCNT	PRESET register is transferred to the counter		-	-
SPI command RESCTL	-	-	Reset to centre position	-
SPI command WCFG	PRESET register is transferred to the EEPROM not affecting the counter		Controller values are transferred to the EEPROM	Configuration is read out the register and written to the EEPROM
Falling edge at ZERO signal [1]	PRESET register is transferred to the counter		-	-
Falling edge at TEACH signal [1] if bit CFG2/TEAEN = 1	Count values are transferred to the PRESET register, then the PRESET register is transferred to the EEPROM		Controller values are transferred to the EEPROM	Configuration is read out the register and written to the EEPROM

[1] If EEPROM is active, see chapter 6.1
[2] If EEPROM is inactive, see chapter 6.1

According to table 24, it is possible to manipulate the counters directly by SPI. For this, registers PRE_ST or PRE_MT have to be written first and then the written content of these registers has to be transferred to the counter by the command RESCNT.

The control signals TEACH and ZERO are debounced in the IC. The relevant function is initiated at the falling edge signal, then no signal changes are considered for the period of $t_{debounce}$. For a clock frequency f_{OSZ} of 40 MHz the period $t_{debounce}$ is about 2.5 ms. The signal TEACH has to be activated by the configuration bit CFG2/TEAEN.

Because counter, controller, and EEPROM are being accessed by several sources the following information has to be taken into account:

- The TEACH signal will be suppressed if there is an active EEPROM access.
- The ZERO signal will be suppressed if there is an active EEPROM access.
- The command RESCNT will be suppressed if there is an active EEPROM access.
- The command WCFG is suppressed if there is an active EEPROM access.
- If the ZERO signal is active while the PRE_ST or the PRE_MT register is written by the SPI, incorrect values can be transferred to the counter.
- If the command WCFG and the TEACH signal are used, the maximum number of write cycles of the EEPROM must be kept in mind.

8 Digital interfaces

8.1 Serial interface SPI

The serial interface SPI will be activated if during the IC's reset the input SEN is kept at H-level. The AM-IP4k operates in slave mode, which means it cannot start to communicate by itself. It is possible to use up to 16 ICs at a single interface bus. The interface is compatible with the most important microcontroller families in SPI mode 0 (16 bit data, MSB first, SCK default low, sampling with rising clock signal edge).

8.1.1 Signals

Table 25: SPI signals

Signal	Meaning	Direction
SCK	Clock With rising edge at SCK the data at MOSI is sampled by the IC With falling edge at SCK the data at MISO is modified by the IC	IN
SEN	Enable Low: Interface is enabled High: Interface is disabled, MISO becomes high-ohmic or is set to nWAIT Rising signal edge: Command is executed	IN
MOSI	Master-OUT / Slave-IN Data input	IN
MISO/nWAIT	Master-IN / Slave-OUT Data output and status signal Please note that at that pin a pull-up resistor is needed!	OUT (Tri-state capable)

During the IC's reset and the waiting time of a synchronous SPI read command, the MISO line is kept at L level (meaning nWAIT).

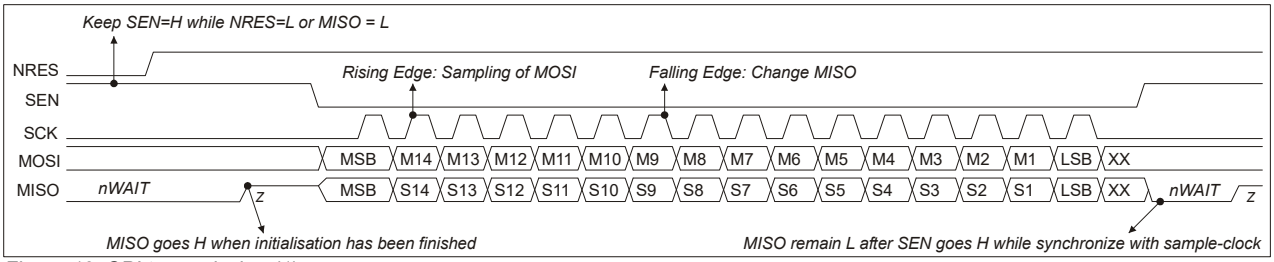


Figure 12: SPI transmission (1)

8.1.2 Protocol

Table 26: SPI protocol

OP Code	Description	Bit at signal MOSI															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		OPC				HWA				DATA							
WRA	Write address	1	0	0	nB	H3	H2	H1	H0	A7	A6	A5	A4	A3	A2	A1	A0
WRD	Write data	1	0	1	nB	H3	H2	H1	H0	D7	D6	D5	D4	D3	D2	D1	D0
RD0/ST	Read bytes 0+1 (2 LSB)	1	1	0	X	H3	H2	H1	H0	A7	A6	A5	A4	A3	A2	0	0
RD1	Read bytes 2+3 (2 MSB)	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X
NOP	Output read register	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

H(3:0): Hardware address, default: '0000', not evaluated, if nB = 0
A(7:0): Register address within the IC
D(7:0): Data word / Write data (Read data appear at MISO)
nB: Broadcast (L-active) 0: Command to all ICs
1: Command to the IC addressed by H(3:0)

Default OP codes

```
WRA = 0x8000+address      WRD = 0xA000+data
RD0 = 0xC000+address      RD1 = 0xE000
NOP = 0x0000
```

Each data transfer is initiated by sending a SPI word by the host processor. A SPI word consists of a 4-bit OP code, a 4-bit hardware address, and 8-bit data. OP codes will only be accepted if the sent hardware address is the same as the stored hardware address of the AM-IP4k. The hardware address of the AM-IP4k is '0000' after a reset. The levels at HWA<3:0> can be read from the IC and taken as the new hardware address by using the command SETHWA. OP codes for reading a register result in the **next** SPI access data output at MISO, regardless of the hardware address in the new SPI word.

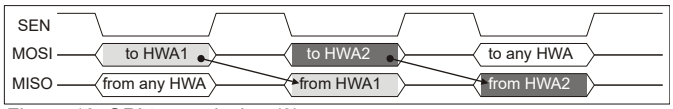


Figure 13: SPI transmission (2)

8.1.3 Register access

The access to the AM-IP4k's registers is done by writing 8 bit and reading 16 bit. The IC's registers are organised in 32 bit. Thus, a 32-bit holding register for read access is implemented in the IC. The data to be read is imported to this holding register by using the SPI word RD0/ST. The data output of the two least significant bytes at MISO is realised during the **next** SPI cycle. The data output of the two most significant bytes at MISO is realised during the SPI cycle following the SPI word RD1 at MOSI. Generally, to read a 32-bit register the commands RD0/ST, RD1, and NOP are executed one after the other. The sequence RD0 – RD1 – RD0 – RD1... can be used to read several registers consecutively. The register address has to be set up first to write a register using the SPI word WRA. Then, the register can be programmed by WRD. A 32-bit register is programmed byte by byte.

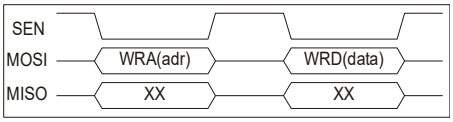


Figure 14: SPI write 8 bit

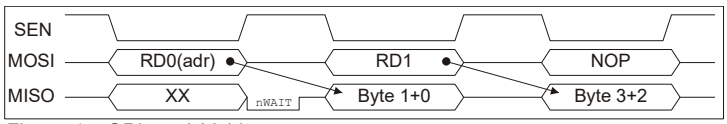


Figure 15: SPI read 32 bit

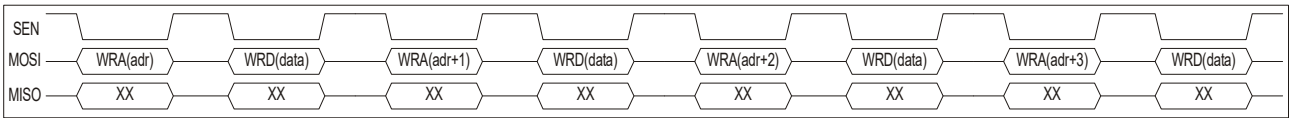


Figure 16: SPI write 32 bit

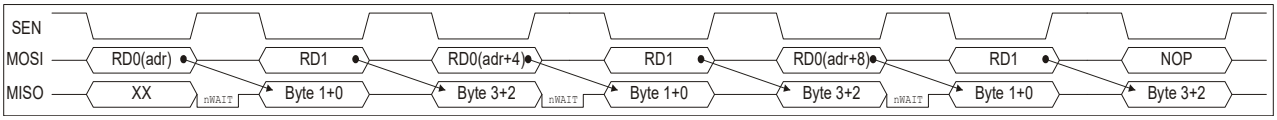


Figure 17: SPI read 3 x 32 bit

8.1.4 SPI – Synchronous / Asynchronous

By executing a read access in any register, the 32-bit register data is imported into the holding register synchronously to the internal process of the IC. The sampling time of the SPI access can be shifted relatively to the sampling time of the ADC by the value SYNC at register CFG2. Thus, it is possible to perform equidistant measurements with only a short down-time. The output MISO is low during the waiting time. The data will be stored immediately after the rising edge at the signal SEN if the bit ASYNC at the register CFG2 is set (asynchronous mode). The time reference to the sampling of the analogue signals is lost. However, higher baud rates can be achieved this way. SYNC can be set to any value to read the registers MVAL, CNT, POSIT, STAT, CTRLG, CTRLO, and ADC. With the default value '00000', there is a short delay between the calculated count value and the data output at the SPI interface. To read the registers CADC, IP1 and IP2, a value of '00100' has to be used.

8.2 SSI interface

The SSI interface of the AM-IP4k will be activated if during the IC's reset the input SEN is kept at the L-level. In order for the AM-IP4k to operate via the SSI interface, the EEPROM **must** contain a valid configuration since the EEPROM contains some basic operating parameters. To operate the interface, the bits SSITO and RING at the register CFGSSI are initialised with the system parameters from EEPROM.

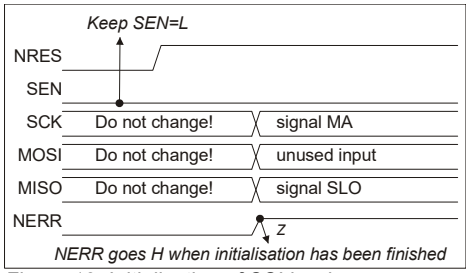


Figure 18: Initialisation of SSI hardware

The register POSIT (see chapter 7.9) is transmitted with a data length of 20 or 32 bit in the data of the SSI protocol. The data contains the value of the interpolation counter (single-turn counter) and of the multi-turn counter. Additionally, two bits are assigned for error information.

Setting the bit RING at the register CFGSSI enables the SSI master to force the repeated transfer of the same value by a continuous clock (SSI ring mode).

ⓘ When using the multi-turn counter the interpolation rate should be set to 256, 128, 64, or 32, since the higher-level interface master usually operates only with binary resolutions.

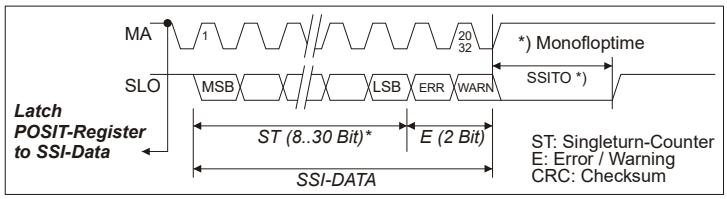


Figure 19: SSI

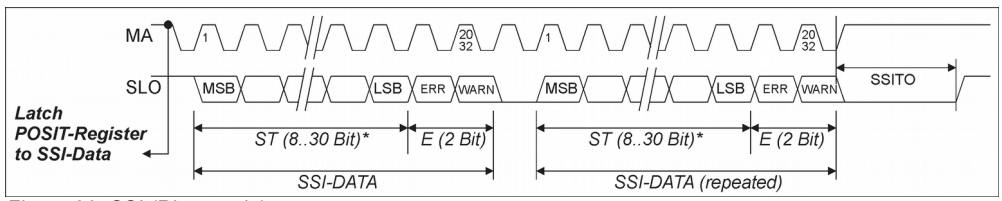


Figure 20: SSI (Ring mode)

Table 27: Register CFGSSI (SSI mode)

Bit	Meaning	Factory setting	User setting
SSITO	SSI timeout	20 µs at 40 MHz	SSITO = (Timeout·f_{OSZ})-3
RING	SSI ring mode	Ring mode	SSI master mode
SSI20	Data length	32 bit	0 for 32 bit / 1 for 20 bit

8.3 EEPROM

The AM-IP4k contains an EEPROM for the permanent storage of the user-specific configuration. After reset it is tested whether the EEPROM is enabled and the content can be read out. The different EEPROM areas are enabled by a stored data word **0x134A at the EEPROM addresses 0x00-0x02.**

Write-access to the EEPROM is realised via an internal interface, which can be executed using the register `EEP`. A reading access of any EEPROM cell is realised via this register too.

The read and write procedures are described in detail in chapter 11.3. It has to be taken into account that if bit `EEPBSY` ist set (EEPROM busy flag), at register `EEP`, the register `EEP` must not be written.

Table 28: EEPROM Addressing

	Register	EEPROM
Data word width	8 bit	16 bit
Address word width	8 bit	8 bit / EEPROM address = register address / 2
Endianess	Little Endian	Little Endian

9 Register

Table 29: Register overview

Register	Access [1]	SPI address	EEPROM address [2]	Annotations
MVAL	R	0x00...0x03	0x00...0x01	Validity of configuration at 0x00 Validity of coefficients SC at 0x01 Validity of coefficients 360 at 0x02
CNT	R	0x04...0x07	0x02...0x03	
STAT/ID/REV	R	0x08...0x0B		
CFG1	R/W	0x0C...0x0F	0x06...0x07	
CFG2	R/W	0x10...0x13	0x08...0x09	
CFG3	R/W	0x14...0x17	0x0A...0x0B	
CFG4	R/W	0x18...0x1B	0x0C...0x0D	
CNTRLG	R/W	0x1C...0x1F	0x0E...0x0F	
CNTRLO	R/W	0x20...0x23	0x10...0x11	
PRE_ST	R/W	0x24...0x27	0x12...0x13	
PRE_MT	R/W	0x28...0x2B	0x14...0x15	
not used	R/W	0x2C...0x2D	0x16	
CFGIUW	R/W	0x2E...0x2F	0x17	Configuration of analogue controller
CFGSSI	R/W	0x30...0x33	0x18...0x19	
CFGLDR	R/W	0x34...0x37	0x1A...0x1B	Configuration Laser diode control
CFGLDR2	R/W	0x38...0x3B	0x1C...0x1D	Configuration Laser diode control 2
MANUFACTURE	!	0x3C...0x3F	0x1E...0x1F	Write-protected
not used	!	0x40...0x47	0x20...0x23	
EEP_DAT	R/W	0x48...0x49		
EEP_ADR / EEP_STAT	R/W	0x4A		
EEP_OPC / EEP_MSB	W	0x4B		
CFGTM	R/W	0x4C..0x4F		Write-protected via TM
CMD	W	0x50...0x51		
TSTCMD (16 bit)	W	0x52...0x53		Write-protected
CFGEEP	R/W	0x54...0x57		
not used	R/W	0x58...0x67	0x2A...0x33	
Abgleich3	!	0x68...0x6B	0x34...0x35	Write-protected
Abgleich2	!	0x6C...0x6F	0x36...0x37	
Abgleich1	!	0x70...0x73	0x38...0x39	
Abgleich0	!	0x74...0x77	0x3A...0x3B	
not used	!	0x78...0x7F	0x3C...0x3F	
not used	R	-	0x40...0x9F	
Koeffizienten_360	R (SPI1)	0x40...0x5F	0xA0...0xBF	
Koeffizienten_SC	R (SPI1)	0x60...0x7F	0xC0...0xDF	
IP-Tabelle (fix)	R (SPI1)	0xC0...0xFF	0xE0...0xFF	Write-protected
POSIT	R	0x80...0x83		
ADC	R	0x84...0x87		
CADC	R	0x88...0x8B		
IP1	R	0x8C...0x8F		
IP2	R	0x90...0x93		
Korrekturwert SC	R	0x94...0x97		
Korrekturwert 360	R	0x98...0x9B		
LDR_OUT	R	0x9C...0x9F		Output value of the laser diode control
SPI-Page = SPI-MSB	R/W	0xFF	-	Available at every SPI page

[1] R: Read-only (Register 32 bit) W: Write-only (Register) R/W: Read/Write (Register)
R (SPI): Read-only via SPI page 1 !: Manufacturer's register. Must not be modified!
[2] The EEPROM address is used for EEPROM reading/writing via the internal interface (register `EEP`).
dark gray: Register loaded from EEPROM during reset
white: EEPROM contains validation identifier 0x134A Fehler: Referenz nicht gefunden

MVAL	Measured value / Trigger value

31:2	1	0
CNT/TVAL	TRG	ERR

Bit	Name	Reset value	Format	Value	Meaning
31:2	CNT/TVAL	0	→ CNT		Measured value; value corresponds to the register CNT respectively to the trigger holding register's content. By reading the value MVAL a trigger holding register may be enabled. → see chapter 7.8
1	TRG	0	Bit	0 1	The measured value corresponds to the current register CNT The measured value corresponds to the content of the trigger holding register
0	ERR	0	Bit	0 1	Measured value is valid. An error occurred. The current measured value and all subsequent values must be discarded. After the removal of the cause of error and the resetting of the error bits (SPI command: RESCNT), it is necessary to cross the reference point again to be able to take measurements using the reference signal! → see chapter 7.6

CNT	Count value

31:2	1	0
CNT	ZSTAT	ERR

Bit	Name	Reset value	Format	Value	Meaning
31:2	CNT	0	Signed		Count value
1	ZSTAT	0	Bit	0 1	Reference mark of the scale has not yet been passed or the count value's reference to the reference mark was lost due to an error. Reference mark of the scale has been passed; AM-IP4k and the incremental scale operate synchronously → see chapter 7.4.3
0	ERR	0	Bit	0 1	Measured value is valid. An error occurred. The current measured value and all subsequent values must be discarded. After the removal of the cause of error and the resetting of the error bits (SPI command: RESCNT), it is necessary to cross the reference point again to be able to take measurements using the reference signal! → see chapter 7.6

POSIT	Position value (Multi-turn + single-turn)

31:2	1	0
POSIT	WARN	ERR

Bit	Name	Reset value	Format	Value	Meaning
31:2	POSIT	0x0000	Unsigned ST Unsigned MT		Position value resulting from multi-turn and single-turn position. → see chapter 7.9
1	WARN	0	Bit	0 1	Measured value is valid. Measured value with a limited accuracy. → see chapter 7.6
0	ERR	0	Bit	0 1	Measured value is valid. An error occurred. The current measured value and all subsequent values must be discarded. After the removal of the cause of error and the resetting of the error bits (SPI command: RESCNT), it is necessary to cross the reference point again to be able to take measurements using the reference signal! → see chapter 7.6

STAT/ID/REV	ASIC identifier / Status

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ASICID				ASICREV				-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EKOVL	-	ZSTAT	TRGOVL	TRGZ	TRGTIM	TRGPIN	ESOFF	ECOFF	ESGAIN	ECGAIN	EABZ	EFAST	ESADC	ECADC	EVLOW

Bit	Name	Reset value	Format	Value	Meaning
31:28	ASICID	0100	Binary	0100	The IC is an AM-IP4k.
27:24	ASICREV	0011	Binary	0011	Silicon revision of the IC
23:16	-	0x00	Binary	-	-
15	EKOVL	0	Binary	0 1	No error in calculating the correction values. The calculated correction value is invalid, caused by the wrong configuration of the correction coefficients. The sensor should be calibrated again.
14	-	0	Bit		-
13	ZSTAT	0	Bit	0 1	Reference mark of the scale has not yet been passed or the count value's reference to the reference mark was lost due to an error. Reference mark of the scale has been passed; the internal counter and the scale operate synchronously. → see chapters 7.4.3, 7.7.3, 7.7.4
12	TRGOVL	0	Bit	0 1	No overflow of the trigger holding register. Overflow of the trigger holding register; trigger event was lost.
11	TRGZ	0	Bit	0 1	Next measured value read from address MVAL was not triggered by the reference signal. Next measured value read from address MVAL was triggered by the reference signal.
10	TRGTIM	0	Bit	0 1	Next measured value read from address MVAL was not triggered by the timer. Next measured value read from address MVAL was triggered by the timer.
9	TRGPIN	0	Bit	0 1	Next measured value read from address MVAL was not triggered by the pin TRG . Next measured value read from address MVAL was triggered by the pin TRG.
8	ESOFF	0	Bit	0 1	No offset error at sine signal. The offset controller of the sine signal has reached its limit caused by a signal offset being too large, an invalid value for the initialisation of the offset controller, or a partially or totally disconnected sensor.
7	ECOFF	0	Bit	0 1	No offset error at cosine signal. The offset controller of the cosine signal has reached its limit caused by a signal offset being too large, an invalid value for the initialisation of the offset controller, or a partially or totally disconnected sensor.
6	ESGAIN	0	Bit	0 1	No amplitude error at sine signal. The gain controller of the sine signal has reached its limit caused by a signal amplitude being too low or by a partially or totally disconnected sensor.
5	ECGAIN	0	Bit	0 1	No amplitude error at cosine signal. The gain controller of the cosine signal has reached its limit caused by a signal amplitude being too low or by a partially or totally disconnected sensor.
4	EABZ	0	Bit	0 1	No error at A, B, Z. The signals at A, B, and Z are invalid because of the input frequency being too high. The monitored frequency depends on the set minimum edge separation t_{pp}. This error will also occur if the interpolation rate or the minimum edge separation are modified. When working in counter mode, the detection of this error will be deactivated automatically.
3	EFAST	0	Bit	0 1	No speed error. The input frequency is too high to generate A/B signals or to detect the direction. The monitored frequency differs to the one of the internal counter and the used square-wave outputs A/B/Z.
2	ESADC	0	Bit	0 1	No ADC error at the sine signal. The A/D converter of the sine signal is over-driven, caused by a signal amplitude being too high. Input signals with a very large offset and a low amplitude at the same time are another source of error.
1	ECADC	0	Bit	0 1	No ADC error at the cosine signal. The A/D converter of the cosine signal is over-driven, caused by a signal amplitude being too high. Input signals with a very large offset and a low amplitude at the same time are another source of error.
0	EVLOW	0	Bit	0 1	No vector error. The signal vector generated from the sine and cosine signal is too small, caused usually by a partially or totally disconnected sensor. Another cause of error are input signals with a very large offset and a low amplitude at the same time.

CFG1 **Configuration 1**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TRI	LKOVL	LOFF	LGAIN	LABZ	LFAST	LADC	LVLOW	HLD	MKOVL	MOFF	MGAIN	MABZ	MFAST	MADC	MVLOW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GAIN		DH			TPP			MODE			IR				

Bit	Name	Reset value	Format	Value	Meaning
31	TRI	0	Bit	0 1	The behaviour of the signals A, B, and Z is determined by the bit HLD in case of error. The signals A,B, and Z get a high-impedance state in case of an error.
30	LKOVL	0	Bit	0 1	Detected errors of the correction value (EKOVL) are not saved. Detected errors of the correction value (EKOVL) are saved.
29	LOFF	0	Bit	0 1	Detected offset errors of the correction value (ESOFF/ECOFF) are not saved. Detected offset errors of the correction value (ESOFF/ECOFF) are saved.
28	LGAIN	0	Bit	0 1	Detected gain errors of the correction value (ESGAIN/ECGAIN) are not saved. Detected gain errors of the correction value (ESGAIN/ECGAIN) are saved.
27	LABZ	0	Bit	0 1	Detected A/B/Z errors of the correction value (EABZ) are not saved. Detected A/B/Z errors of the correction value (EABZ) are saved.
26	LFAST	0	Bit	0 1	Detected speed errors of the correction value (EFAST) are not saved. Detected speed errors of the correction value (EFAST) are saved.
25	LADC	0	Bit	0 1	Detected ADC errors of the correction value (ESADC/ECADC) are not saved. Detected ADC errors of the correction value (ESADC/ECADC) are saved.
24	LVLOW	0	Bit	0 1	Detected vector errors of the correction value (EVLOW) are not saved. Detected vector errors of the correction value (EVLOW) are saved.
23	HLD	1	Bit	0 1	The behaviour of the signals A, B, and Z is not defined in case of error. The signals A, B, and Z are not modified in case of error.
22	MKOVL	1	Bit	0 1	The detection of errors of the correction value (EKOVL) is deactivated. The detection of errors of the correction value (EKOVL) is activated.
21	MOFF	1	Bit	0 1	The detection of offset errors (ESOFF/ECOFF) is deactivated. The detection of offset errors (ESOFF/ECOFF) is activated.
20	MGAIN	1	Bit	0 1	The detection of gain errors (ESGAIN/ECGAIN) is deactivated. The detection of gain errors (ESGAIN/ECGAIN) is activated.
19	MABZ	1	Bit	0 1	The detection of A/B/Z errors (EABZ) is deactivated; the IC operates in counter mode. The detection of A/B/Z errors (EABZ) is activated; the IC operates in square-wave mode.
18	MFAST	1	Bit	0 1	The detection of speed errors (EFAST) is deactivated. The detection of speed errors (EFAST) is activated.
17	MADC	1	Bit	0 1	The detection of ADC errors (ESADC/ECADC) is deactivated. The detection of ADC errors (ESADC/ECADC) is activated.
16	MVLOW	1	Bit	0 1	The detection of vector errors (EVLOW) is deactivated. The detection of vector errors (EVLOW) is activated.
15:14	GAIN	00	Binary	00 01 10 11	Nominal amplitude 1000 mV Nominal amplitude 500 mV Nominal amplitude 250 mV Nominal amplitude 75 mV
13:11	DH	001	Unsigned	DH	Threshold value of the digital hysteresis. A value of “0” deactivates the digital hysteresis.→ see chapter 7.4.2
10:8	TPP	001	Unsigned	TPP	Minimum edge separation $t_{pp} = 2^{TPP}/f_{OSZ}$ → see chapter 7.4.2, 7.5
7:5	MODE	000	Binary	000 001 010 011 100 111	Standard mode ABZ Sensor adjustment 1 Sensor adjustment 2 Sensor adjustment Z MC mode / DSP Calibration mode → see chapter 7.7
4:0	IR	00000	Binary	IR	Configuration of the interpolation rate → see chapter 7.4.1

CFG2	Configuration 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	LP		DISMON	DISV0	DISKSC	DISK360	TEAEN	TRGSLP	PHBER	PH					

15	14	13	13	11	10	9	8	7	6	5	4	3	2	1	0
ASYNC	SYNC							IRDIV2			OFFSCTL		GAINCTL		DISCTL

Bit	Name	Reset value	Format	Value	Meaning
31	ENA_AJ	0	Bit	0 1	Anti jitter is deactivated. Anti jitter is activated.
30:29	LP	00	Binary	00 01 10 11	The analogue low-pass filter is deactivated. The analogue low-pass filter's cut-off frequency (-1dB) of 250 kHz. The analogue low-pass filter's cut-off frequency (-1dB) of 75 kHz. The analogue low-pass filter's cut-off frequency (-1dB) of 10 kHz.
28	DISMON	0	Bit	0 1	The pins SMON and CMON are active. The pins SMON and CMON are inactive (Power saving mode).
27	DISV0	0	Bit	0 1	The pin V1P1 is active. The pin V1P1 is inactive (Power saving mode).
26	DISKSC	0	Bit	0 1	Periodic harmonic wave correction is activated. Periodic harmonic wave correction is deactivated.
25	DISK360	0	Bit	0 1	Position error correction is activated. Position error correction is deactivated.
24	TEAEN	0	Bit	0 1	Teach function is inactive. Teach function is active. → see chapter 7.10.
23	TRGSLP	0	Bit	0 1	A falling edge at pin TRG initiates the measured value's transfer to the trigger holding register. A rising edge at pin TRG initiates the measured value's transfer to the trigger holding register.
22	PHBER	0	Bit	0 1	The setting range of the phase correction potentiometer is ± 5°. The step size is 0.156°. The setting range of the phase correction potentiometer is ± 10°. The step size is 0.313°.
21 : 16	PH	000000	Signed	-32 PH +31	The maximum phase shift is negative. The setting value of the phase correction potentiometer. The maximum phase shift is positive.
15	ASYNC	0	Bit	0 1	The data to be read is transferred synchronously with the internal sequence to a 32 bit holding register by the SPI word RD0/ST. With the value of SYNC it is possible to shift the transfer's point in time relative to the sampling time. The data to be read is transferred asynchronously with the internal sequence to a 32 bit holding register by the SPI word RD0/ST. The value of SYNC is not evaluated.
14:8	SYNC	0000000	Unsigned		Shift of the SPI read-access relative to the sampling time. To read the registers IP1, IP2, CADC, and to read the SPI page 1 a value of 64 (decimal) has to be used.
7:5	IRDIV2	000	Binary	Div	Configuration of IR divider see Chapter 7.4.1
4:3	OFFSCTL	01	Binary	00 01 10 11	Maximum settling time of the offset controller. This configuration has to be selected if the sensor signal has a low input frequency or is overlaid by noise or the phase between the sine and the cosine signal cannot be adjusted completely by the phase correction potentiometer. Reduction of the settling time of the offset controller by a factor of about 2. Reduction of the settling time of the offset controller by a factor of about 4. Reduction of the settling time of the offset controller by a factor of about 8.
2:1	GAINCTL	01	Binary	00 01 10 11	Maximum settling time of the gain controller. This configuration has to be selected if the sensor signal has a low input frequency or is overlaid by noise or the phase between the sine and the cosine signal cannot be adjusted completely by the phase correction potentiometer. Reduction of the settling time of the gain controller by a factor of about 2. Reduction of the settling time of the gain controller by a factor of about 4. Reduction of the settling time of the gain controller by a factor of about 8.
0	DISCTL	0	Bit	0 1	The internal controller for gain and offset is activated. The internal controller for gain and offset is deactivated.

CFG3 **Configuration 3**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	VT		T							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MXSHR	-	-	PHIOUTZ	ZDEL2		ZDEL	DISZ	ZMODE		Z4	-				

Bit	Name	Reset value	Format	Value	Meaning
31	-	0	Binary	-	-
30	SE_VR_int	0	Binary	0 1	Inputs SINN, COSN used Internal reference replaces inputs SINN, COSN for single-ended
29	SE_halb	0	Binary	0 1	No resistance divider before INST-AMP (instrumentation amplifier) Switches ½ resistance divider before INST-AMP (instrumentation amplifier)
28	SE_amp2	0	Binary	0 1	Normal amplification at SUM_AMP Double amplification at SUM_AMP, goal: to counterbalance SE_halb
27:26	-	0	Binary	-	-
25:24	VT	00	Binary	00 01 10 11	$f_{VT} = f_{OSZ}/2^6$ $f_{VT} = f_{OSZ}/2^{10}$ $f_{VT} = f_{OSZ}/2^{14}$ $f_{VT} = f_{OSZ}/2^{16}$
23:16	T	0x00	Unsigned	T	Timer's time constant. $t_{Timer} = (T+1)/f_{VT}$. If VT = T = 0, the timer will be deactivated. → see chapter 7.8
15	MXSHR	1	Bit	0 1	Coefficient scale 16 bit Coefficient scale 18 bit
14	PHRENA	0	Bit	0 1	Phase correction from CFG2/PHBER and CFG2/PH is disregarded. Integrated Phase correction is activated
13	ABMX	0	Bit	0 1	Signal A/B swap at output. PinA = A, PinB= B PinA = B, PinB= A
12	PHIOUTZ	0	Bit	0 1	The read register PHI refers to the sine and cosine signal. 0° correspond to sine zero crossing and cosine maximum. The read register PHI refers to the set reference point position ZPOS2. 0° correspond to ZPOS2
11-10	ZDEL2	00	Unsigned	00 01..11	No additional delay of the reference point signal Additional internal delay of the reference point signal of ZDEL2 x CLKs
9	ZDEL	0	Bit	0 1	Default value Additional internal delay of the reference point signal of $64/f_{OSZ}$.
8	DISZ	0	Bit	0 1	Reference point processing is activated. The activation (DISZ switches from 1 to 0) requires 100µs. Reference point processing at channel 1 is deactivated.
7:6	ZMODE	00	Binary	00 01 10 11	Reference point mode incremental Reference point mode trigger Reference point mode adjustment Z Reference point mode distance coded → see chapters 7.4.3, 7.7.3, 7.8
5	Z4	0	Bit	0 1	Width of the index signal Z is 1 increment = ¼ period Width of the index signal Z is 4 increments = 1 period → see chapter 7.4.3
4:0	-	00000	Binary	-	-

CFG4	Configuration 4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	Zahnzahl												

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZPOS2															

Bit	Name	Reset value	Format	Value	Meaning
31:29	-	000	Binary	-	-
28:16	Zahnzahl	0x000	Unsigned	ZZahl	Number of teeth for disc correction
15:0	ZPOS2	0x0000	Unsigned	ZPOS2	Configuration of the analogue reference point position referring to the sine signal. Position of the reference point = ZPOS2 / IRATE * 360° (with IRATE = basic interpolation rate) → see chapter 7.4.3

CFGSSI	Configuration SSI

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	SSI20	RING	SSITO											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MTBIT		GRAY	STBIT					-	-	-	-	-	-	-	-

Bit	Name	Reset value	Format	Value	Meaning
31:30	-	00	Binary	-	-
29	SSI20	1	Bit	0 1	32 bit SSI data 20 bit SSI data → see chapters 7.9, 8.2
28	RING	1	Bit	0 1	SSI ring mode deactivated. SSI ring mode activated. → see chapter 8.2
27:16	SSITO	797 (decimal)	Binary	SSITO	Set-up of the SSI timeout parameter to 1µs...20 µs. Timeout = (SSITO+3)/f_{OSZ} respectively SSITO = (Timeout·f_{OSZ})-3 For example: f_{OSZ} = 40MHz → SSITO = 37 (1µs) … 797 (20µs) → see chapter 8.2
15:14	MTBIT	00	Binary	00 01 10 11	0 bit multi-turn counter at the position data 8 bit multi-turn counter at the position data 12 bit multi-turn counter at the position data 16 bit multi-turn counter at the position data → see chapter 7.9 and table 23
13	GRAY	0	Bit	0 1	Position data (Multi-turn and single-turn counter) is binary coded. Position data (Multi-turn and single-turn counter) is gray coded.
12:8	STBIT	30 (decimal)	Binary	STBIT	Word width of the single-turn value within the position data in bit, range 8...30 bit. The number of the bits transmitted is shown in table 23.
7:0	-	0x00	Binary	-	-

CFGIUW	Configuration analogue controller

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	LD_DEL	ENA_REGA	R_REG		CMP_OPR	ENA_OPLD	ENA_REGD	-	-	-	-	-

Bit	Name	Reset value	Format	Value	Meaning
31:12	-	0x00000	Binary	-	-
11	LD_DEL	0	Bit	LD_DEL	Switch of the frequency compensation (DELAY)
10	ENA_REGA	0	Bit	0 1	Analogue controller deactivated Analogue controller activated
9:8	R_REG	00	Binary	R_REG	Summing resistors of the controller input
7	CMP_OPR	0	Bit	0 1	Lower frequency compensation Higher frequency compensation
6	ENA_OPLD	0	Bit	0 1	Output OPA deactivated LD output active
5	ENA_REGD	0	Bit	0 1	Digital controller deactivated Digital controller active
4:0	-	00000		-	-

CFGLDR	Configuration sum signal control

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ENA	INV	CONT	DC	MUX	D[6:4]			D[3:0]				OFFS[7:4]			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFS[3:0]				W[11:8]				W[7:0]							

Bit	Name	Reset value	Format	Value	Meaning
31	ENA	0	Bit	0 1	Digital controller off Digital controller on
30	INV	0	Bit	0 1	Initial value normal Initial value inverted
29	CONT	0	Bit	0 1	Control once per turn Continuous control
28	DC	0	Bit	0 1	Normal controller function Output of DC value (= reference variable)
27	MUX	0	Bit	0 1	Square of the absolute value BQ as input variable of the controller invalid
26:20	D	0000000	Unsigned	D	D-share of the PID controller
19:12	OFFS	0x00	Signed	OFFS	Initial value of the offset
11:0	W	0x000	Unsigned	W	Reference variable of the controller

CFGLDR2	Configuration sum signal control 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAX								GAIN							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I								P							

Bit	Name	Reset value	Format	Value	Meaning
31:24	MAX	0x00	Unsigned	MAX	Maximum value of the initial value's limit
23:16	GAIN	0x00	VZ+OneHot	0xxxxxxx 1xxxxxxx y0000000	Amplification Attenuation Factor 2nd power (OneHot)
15:8	I	0x00	Unsigned	I	I-share of the PID controller
7:0	P	0x00	Unsigned	P	P-share of the PID controller

PRE_ST	Preset value single-turn

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRE_ST(31:16)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRE_ST(15:0)															

Bit	Name	Reset value	Format	Value	Meaning
31:0	PRE_ST	0	Unsigned	PRE_ST	Preload-value of the single-turn counter → see chapter 7.10

PRE_MT	Preset value multi-turn

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRE_MT															

Bit	Name	Reset value	Format	Value	Meaning
31:16	-	0x0000	Binary	-	-
15:0	PRE_MT	0	Signed	PRE_MT	Preload-value of the multi-turn counter → see chapter 7.10

CNTRLG	Controller: Gain correction value

For writing the bits (26:16) the bits, (23:16) have to be written first. By writing the bits (26:24) afterwards the complete correction value is updated at the register. For writing the bits (10:0) the bits, (7:0) have to be written first. By writing the bits (10:8) afterwards the complete correction value is updated at the register. Please note that with the signal control being activated the correction values are updated automatically by the IC.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	CNTRLG_S										

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	CNTRLG_C										

Bit	Name	Reset value	Format	Value	Meaning
26:16	CNTRLG_S	0x400	Unsigned	CNTRLG	CADC_S = [ADC_S + CNTRLO_S] · (0.5 + CNTRLG_S/2048) CADC_C = [ADC_C + CNTRLO_C] · (0.5 + CNTRLG_C/2048)
				0x000	Minimum value; the offset corrected ADC values of the sine signal are multiplied by 0.5.
10:0	CNTRLG_C	0x400	Unsigned	0x400	Mean value; the offset corrected ADC values of the sine signal are multiplied by 1.0.
				0x7FF	Maximum value; the offset corrected ADC values of the sine signal are multiplied by 1.5.

CNTRLO	Controller: Offset correction value

For writing the bits (31:16), the bits (23:16) have to be written first. By writing the bits (31:24) afterwards the complete correction value is updated at the register. If the value to be written is out of the range of -683 to +682, the correction register will not be updated and the bit ESOFF will be set at the register STAT/ERR.
For writing the bits (15:0), the bits (7:0) have to be written first. By writing the bits (15:8) afterwards the complete correction value is updated at the register. If the value to be written is out of the range of -683 to +682, the correction register will not be updated and the bit ECOFF will be set at the register STAT/ERR. Please note that with the signal control being activated the correction values are updated automatically by the IC.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CNTRLO_S															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNTRLO_C															

Bit	Name	Reset value	Format	Value	Meaning
31:16	CNTRLO_S	0x0000	Signed	CNTRLO	CADC_S = [ADC_S + CNTRLO_S] · (0.5 + CNTRLG_S/2048) CADC_C = [ADC_C + CNTRLO_C] · (0.5 + CNTRLG_C/2048)
				0xFD55	Minimum value -682
15:0	CNTRLO_C	0x0000	Signed	0x0000	Mean value 0; no offset correction
				0x02AA	Maximum value +683

CMD	Command

7	6	5	4	3	2	1	0
TRGCAL	-	SETHWA	WCFG	RESIC	CLRZ	RESCTL	RESCNT

Bit	Name	Reset value	Format	Value	Meaning
7	TRGCAL		Bit write-only	1	The registers needed for calibration are updated. The registers are updated too if the trigger (pin TRG) is active.
6	-		Bit write-only	-	-
5	SETHWA		Bit write-only	1	The pins HWA3, HWA2, HWA1, and HWA0 are read as a hardware address in the IC. If several ICs are supposed to be operated on one interface, this command has to be sent first to all the ICs connected.
4	WCFG		Bit write-only	1	The content of the registers CFG1, CFG2, CFG3, CNTRLG, and CNTRLO is transferred to the EEPROM. The content of the register CFGSSI is not transferred to the EEPROM.
3	RESIC		Bit write-only	1	The IC is reset and reconfigured.
2	CLRZ		Bit write-only	1	The status bit ZSTAT is reset. For the reference point modes “Adjustment ZPOS2” and “Distance coded” a new analysis is started.
1	RESCTL		Bit write-only	1	The internal controller for gain and offset is reset, i.e. the correction values for gain and offset are set to the centre of their range of values.
0	RESCNT		Bit write-only	1	The count value is loaded with the content of the register PRE_ST. The multi-turn counter is loaded with the value from PRE_MT. All error flags at the status register are reset. The status bit ZSTAT is reset. For the reference point modes “Adjustment ZPOS2” and “Distance coded” a new analysis is started. → see chapter 7.10

ADC	ADC values

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADC_S															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC_C															

Bit	Name	Reset value	Format	Value	Meaning
31:16	ADC_S	-	Signed	0xF800	Minimum value -2048; corresponds to a differential voltage of about -787 mV at the input of the instrumentation amplifier (@GAIN=00).
				0x0000	Mean value 0; corresponds to a differential voltage of about 0 mV at the input of the instrumentation amplifier.
15:0	ADC_C	-	Signed	0x07FF	Maximum value +2047; corresponds to a differential voltage of about +787 mV at the input of the instrumentation amplifier (@GAIN=00).

CADC	Corrected ADC values

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VZ(CADC_S)	0	Abs(CADC_S)													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VZ(CADC_C)	0	Abs(CADC_C)													

Bit	Name	Reset value	Format	Value	Meaning
31	VZ(CADC_S)	-	Bit	0 1	Corrected sine ADC value ≥ 0 Corrected sine ADC value < 0
29:16	Abs(CADC_S)	-	Unsigned	0 0xFFF	Corrected sine ADC value (absolute value) Minimum value Maximum value
15	VZ(CADC_C)	-	Bit	0 1	Corrected cosine ADC value ≥ 0 Corrected cosine ADC value < 0
13:0	Abs(CADC_C)	-	Unsigned	0 0xFFF	Corrected cosine ADC value (absolute value) Minimum value Maximum value

Bit	Name	Reset value	Format	Value	Meaning
31:16	CADC_S	-	Sign + absolute value	CADC	Corrected sine ADC value `CADC_S = [ADC_S + CNTRLO_S] · (0.5 + CNTRLG_S/2048)`
15:0	CADC_C	-	Sign + absolute value	CADC	Corrected cosine ADC value `CADC_C = [ADC_C + CNTRLO_C] · (0.5 + CNTRLG_C/2048)`

IP1	Interpolation register 1 – Angle value / Speed

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DPHI															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHI															

Bit	Name	Reset value	Format	Value	Meaning
31:16	DPHI	-	Signed	DPHI	The value `DPHI` is the difference of the sine signal's and the cosine signal's phase angle between two samplings. The range of values depends on the set basic interpolation rate. This value indicates the speed of the measuring system. f_{Input} = DPHI/(96 · IRATE)·f_{OSZ}
15:0	PHI	-	Unsigned	0x0000 IRATE-1	The phase angle of the sine and cosine signal is 0°. The phase angle of the sine and cosine signal is 360°- ε. The maximum value depends on the set interpolation rate. The reference value (0°) can be shifted by the bit `CFG3/PHIOUTZ`.

IP2	*Interpolation register 2 – Angle value / Controller value*

In calibration mode (`CFG1/MODE` = `111`) a quadrant count value is stored in the bits 31:16 of the register IP2 via trigger or SPI command `TRGCAL`.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BQ															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHI															

Bit	Name	Reset value	Format	Value	Meaning
31:16	BQ	-	Unsigned	BQ	The value BQ contains the deviation of the gain and offset controller from the setpoint value. If offset and gain are adjusted completely, this register will be a value of 321.
15:0	PHI	-	Unsigned	0x0000 IRATE-1	The phase angle of the sine and cosine signal is 0° The phase angle of the sine and cosine signal is 360° - ε The maximum value depends on the set interpolation rate.

EEP	EEPROM interface

Read access

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-				INIT	-	AUT	RSV	EEPVALID	EER	EWR	EEPBSY	EEPLOCK

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EEPDAT															

Bit	Name	Reset value	Format	Value	Meaning
24	INIT		Bit	1	This bit is reserved for test purposes.
22	AUT	0	Bit		This bit is reserved for test purposes.
21	RSV	0	Bit		This bit is reserved for test purposes.
20	EEPVALID	0/1	Bit	0 1	Validation identifier 0x134A at address 0x00 was not found. Validation identifier 0x134A at address 0x00 was found. The EEPROM content was loaded in the related registers after a reset.
19	EER	0	Bit	0 1	No EEPROM reset command active EEPROM reset command active
18	EWR	0	Bit	0 1	No EEPROM read access active EEPROM read access active
17	EEPBSY	0	Bit	0 1	No EEPROM access active EEPROM access active; any further command must not be sent to the EEPROM
16	EEPLOCK	0	Bit	0 1	EEPROM available EEPROM locked
15:0	EEPDAT	0x0000	Binary		Read EEPROM data

Write acess

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	EEPOPC			EEPADR							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EEPDAT															

Bit	Name	Reset value	Format	Value	Meaning
26:24	EEPOPC	000	Binary	000 001 010 100 others	EEP-OPCode; **Writing these bits triggers an EEPROM access**. The register must not be written if bit `EEPBSY` is set. `EEPADR` and `EEPDAT` have to be valid. NOP – No action WRITE – Write 16 bit READ – Read 16 bit ERASE – Delete 16 bit Undefined behaviour. The EEPROM content might be lost → see chapters 8.3, 11.3
23:16	EEPADR	0x00	Binary		EEPROM address; to delete, to write, or to read the EEPROM the address has to be written to this register before activating the OP codes. The register must not be written if bit `EEPBSY` is set.
15:0	EEPDAT	0x0000	Binary		EEPROM data; to program the EEPROM the data has to be written to this register before activating the OP codes. The register must not be written if bit `EEPBSY` is set.

10 Characteristic values

Table 30: Absolute limit values

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
VDDA	Supply voltage analogue			3.60	V
VDD	Supply voltage digital			3.60	V
T	Operating temperature	-40		125	°C
TS	Storage temperature	-55		150	°C
V(AIN)	Voltage at the analogue inputs	-0.3		VDDA+0.3	V
V(DIN)	Voltage at the digital inputs	-0.3		VDD+0.3	V
ESD	ESD resistance (HBM)			2	kV

Table 31: Operating conditions

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
VDDA	Supply voltage analogue	3.15	3.30	3.45	V
VDD	Supply voltage digital	3.15	3.30	3.45	V
I(VDDA)	Current consumption analogue		10		mA
I(VDD)	Current consumption digital f_{OSZ} (internal)		14		mA
I(VDD)	Current consumption digital f_{OSZ} (external)		$0.29 \cdot f_{OSZ} + 5.1$		mA
T	Operating temperature	-40		125	°C

Table 32: Characteristic values clock/reset

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
f_{OSZ} (internal)	Internal clock: Frequency		40		MHz
f_{OSZ} (external)	External clock: Frequency			40	MHz
TH/TL	External clock: Duty cycle	40	50	60	%
t_{INIT}	Initialization period Period between `NRES` rising and Ready (`MISO`,`NERR`)		40	50	ms

Table 33: Characteristic values interpolation

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
f_{IP}	Input frequency	0		220	kHz
IRATE	Interpolation rate	4		4096	Increments
CTRL(A)	Amplitude control range	60		120	%VINNOM[2)]
CTRL(O)	Offset control range	-15		15	%VINNOM[2)]
VTH(INP)	Threshold vector monitoring		30		%VINNOM[2)]
EABS	Absolute angle error[1)]		±0.75	1.0	Increments
EDIFF	Differential angle error[1)]		±0.50		Increments
tpp	Minimum edge separation A/B	$1/f_{OSZ}$		$128/f_{OSZ}$	ns
tp(TRG)	Pulse width of trigger signal	$3/f_{OSZ}$			ns
tp(Teach)	Pulse width of zero/teach signal	$40000/f_{OSZ}$			ns
td(CNT)	Delay time analogue input to `CNT` or `POSIT` (`@DISLP=1`)		$90/f_{OSZ} + 100$		ns
td(ABZ)	Delay time analogue input to A/B (`@DISLP=1`)		$122/f_{OSZ} + 100$		ns

[1)] In case of adjusted phase between sine and cosine.
[2)] Nominal value of the differential voltage of SINP-SINN or COSP-COSN.

Table 34: Digital characteristic values

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
VOH	Output voltage H	80			%VDDIO
VOL	Output voltage L			0.4	V
VIH	Input voltage H	70			%VDDIO
VIL	Input voltage L			30	%VDDIO
I(DIG1)	Output current digital			6	mA
I(DIG2)	Output current digital at `MISO` and `NERR`			12	mA
R(PU)	Internal pull-up resistors	90		210	KΩ
R(PD)	Internal pull-down resistors	75		250	KΩ

Table 35: Analogue characteristic values

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
Z(AIN)	Input impedance		1GΩ||8pF		
Gain	Gain (as per table 10) @1kHz	97	100	103	%
fg	Cut-off frequency (as per table 13) @`CFG2/DISLP` = 0	90	100	110	%
fg_{bypass}	Cut-off frequency @`CFG2/DISLP` = 1	400			kHz
fg_{MATCH}	Deviation of the cut-off frequencies between the channels	-1	0	+1	%
V(AIN)	Voltage at the analogue inputs	0..65		VDDA-0.45	V
CMIR	Common-mode input voltage → Figure 6		2.5		V
CMRR	Common-mode rejection (@ f < 1kHz, `CFG1/GAIN` = 11)	65			dB
V(V0)	Voltage at Pin `V1P1` / DC voltage at `SMON/CMON`	1.08	1.1	1.12	V
VMON	AC voltage at `SMON/CMON` @ nominal amplitude		1.27		V_{pp}
I(V0)	Output current at Pin `V1P1`			1	mA
CL(V0)	Capacitive load at Pin `V1P1`			300	pF
VTH(REF)	Switching threshold of the reference point comparator[2)]	-1		1	mV
VH(REF)	Hysteresis of the reference point comparator[2)]		15		%VINNOM[1)]
I(OUTX)	Output current at Pin `SMON/CMON`			0.05	mA
CL(OUTX)	Capacitive load at Pin `SMON/CMON`			50	pF
φK1	Setting range phase correction (@ `CFG2/PHBER` = 0)	± 4.5	± 5	± 5.5	°
φK2	Setting range phase correction (@ `CFG2/PHBER` = 1)	± 9	± 10	± 11	°

[1)] Nominal value of the differential voltage of SINP-SINN or COSP-COSN.
[2)] Differential voltage of REFP-REFN.

Table 36: Characteristic values EEPROM

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
$t_{READEEP}$	Reading time	20		85	us
$t_{PROGEEP}$	Programming time / Deletion time	4		9	ms
$t_{RETENTIONEEP}$	Data retention @ T < 85°	10			Years
$N_{ProgEEP}$	Programming cycles @ T = 25° @ T = 125°	10^4 10^3			

Table 37: Characteristic values SSI interface

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
f_{MA}	Clock frequency @ f_{OSZ} ≥ 4MHz @ f_{OSZ} ≥ 8MHz @ f_{OSZ} ≥ 10MHz @ f_{OSZ} ≥ 20MHz			2 3 4 5	MHz
t_D(MISO)	Delay time `MA` rising to `SLO`			25	ns
$t_{TIMEOUT}$	Time-out → `CFGSSI/SSITO`	1		20	µs

11 Application note

11.1 Circuitry

As the AM-IP4k contains two fast A/D converters, the same design guidelines shall be applied as with the application of A/D converters. Concerning standard sensors, it should be taken into account, that the power supply quality influences the accuracy of measurement. If necessary, additional LC combinations for sensor power supply and for VDDA shall be provided. Supply voltages and ADC reference voltages are connected according to the table 38; and unused inputs and outputs according to table 39.

Table 38: IC connection voltages

Pin	Connection
VSSA	Analogue ground plane
VSS, VSSIO, Exposed Pad	Digital ground plane
VDDA	Analogue voltage supply 3.3 V Block capacitor 100 nF against VSSA
VDD, VDDIO	Digital voltage supply 3.3 V Block capacitor 100 nF against VSS/VSSIO
VRL, VRM, VRH, V1P1	Block capacitor 10 nF || 2.2 µF against VSSA

Table 39: Connection of unused in- and outputs

Pin	Connection, if unused
NRES	Pull-up 10k against VDDIO
CLK_CKSEL	VSS
SINN, COSN, REFN	V1P1
REFP	VDDA
TEACH	VDDIO
ZERO	VDDIO
MISO/SLO	Pull-Up 10k against VDDIO
MOSI/SLI	VSSIO
SCK/MA	VSSIO
SEN	VDDIO
NERR	Pull-Up 10k against VDDIO
TM/TM2	VSS

Furthermore:

- All block capacitors shall be closely connected to the pad.
- Separate ground planes for VSSA and VSS/VSSIO are needed.
- When using the SPI with high data rates serial resistors of 22...33 Ω each at MOSI, MISO, SCK, and SEN are beneficial.
- The digital outputs A, B, and Z are designed for an output current of max. 12 mA. An external driver IC is required to realise a differential RS422 interface. In case of an error, these outputs can be set up to a tri-state behaviour. Depending on the application and the configuration pull-up resistors are needed.
- The sensor manufacturer's instructions apply to additional terminating resistors between SINP and SINN respectively between COSP and COSN.
- Single-ended sensors are usually connected to the inputs SINP and COSP. For this purpose, the DC reference level of the IC has to correspond with that of the sensor.
- The signal V1P1 can be used as DC reference level. The current carrying capacity of this pin is 1 mA. Attention should be paid to a short and low-capacitance wiring. It is possible to envisage an operational amplifier.
- For a reliable operation all IC inputs have to be connected in a defined way. Internal pull-up resistors only prevent unpredictable IC behaviour as inputs are open.

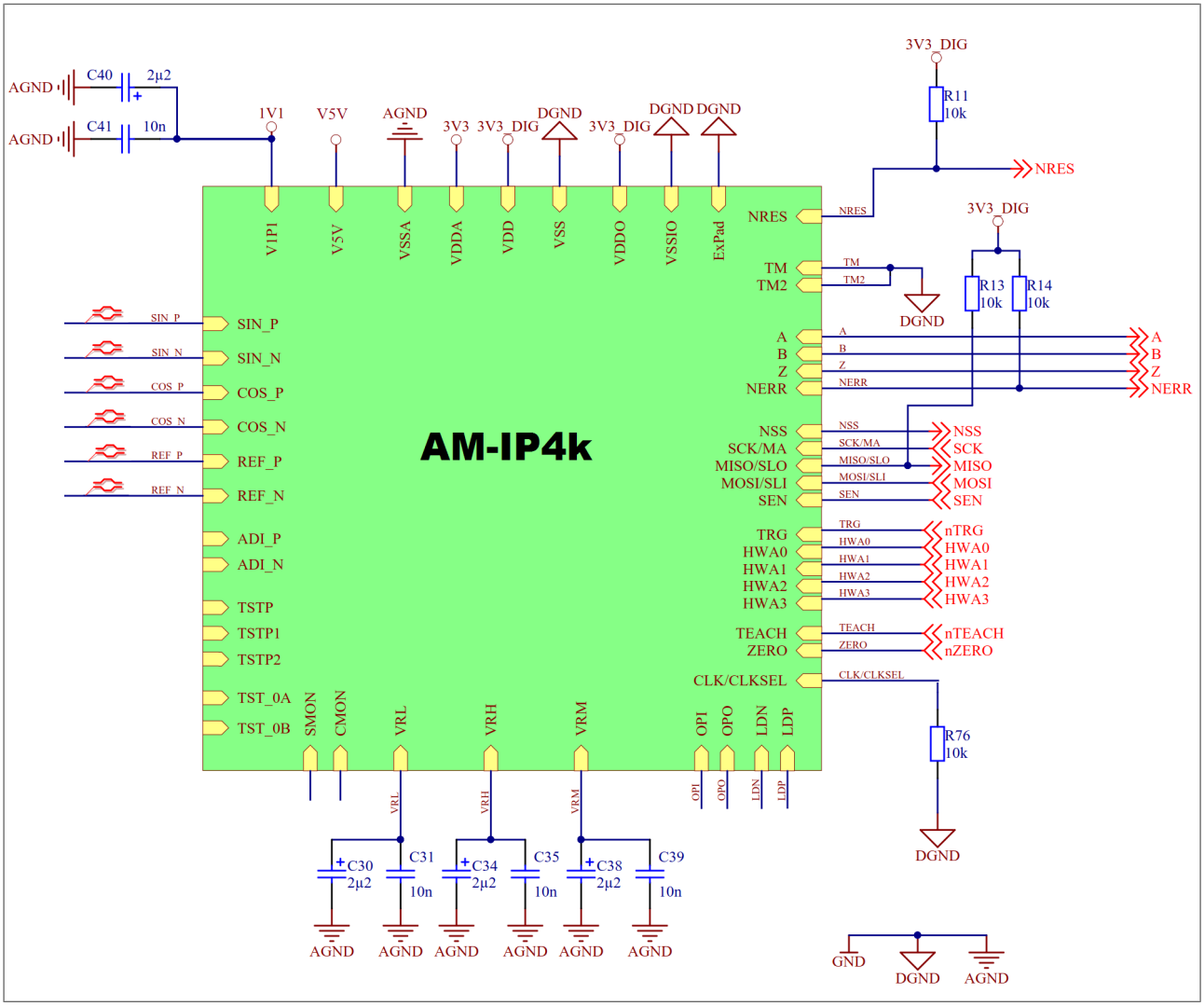


Figure 21: Minimum circuit of the AM-IP4K

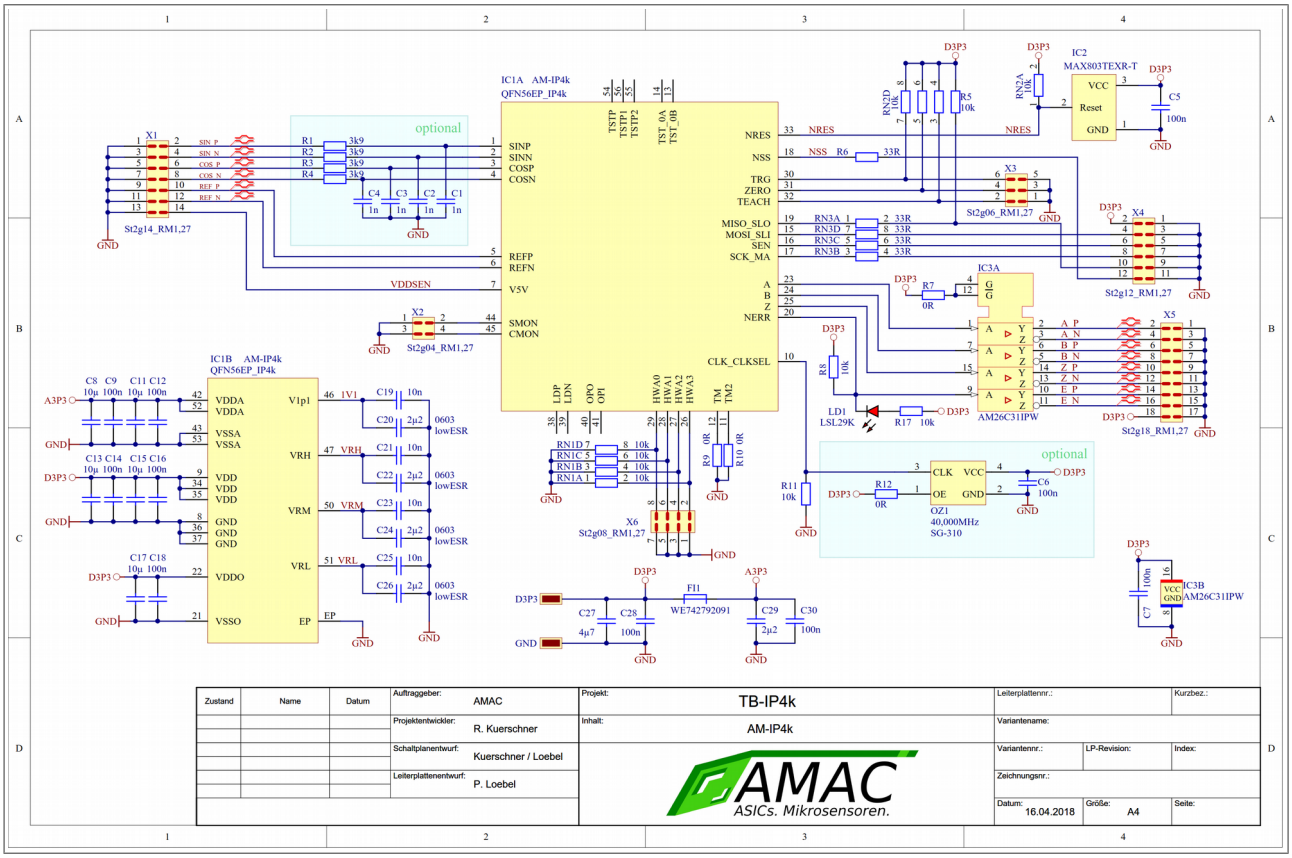


Figure 22: AM-IP4k recommended circuit

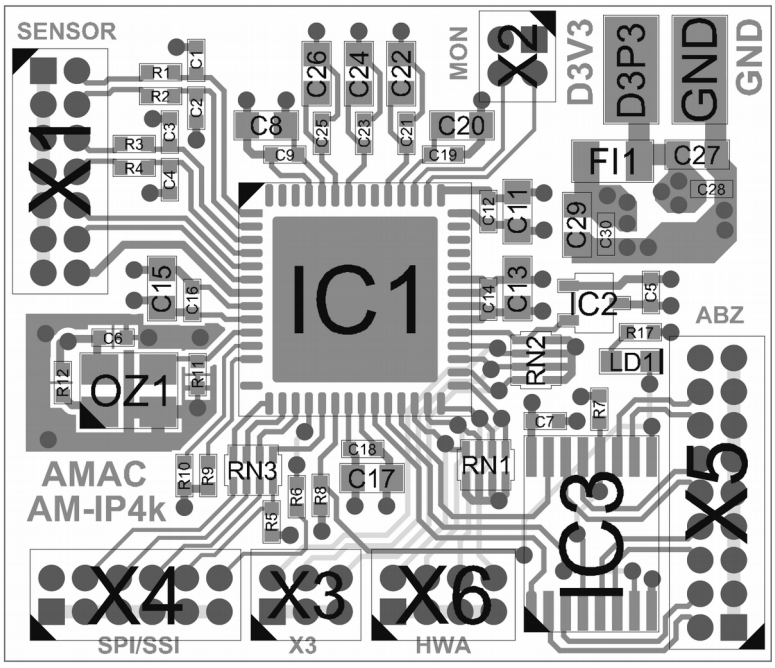


Figure 23: AM-IP4k recommended PCB Layout

11.2 Connecting different types of sensors

The design of the analogue input circuit depends on the type of the sensor connected. The following figures show examples of the connection of different sensor types.

Sensor with differential output signals

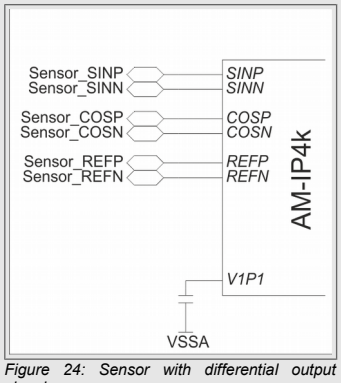


Figure 24: Sensor with differential output signals

- The sensor amplitude and the nominal amplitude of the AM-IP4k are harmonised by the configuration bits `GAIN(1:0)`.
- The reference level `V1P1` is generated **internally**.

Sensor with a nominal amplitude > 1V_{pp}

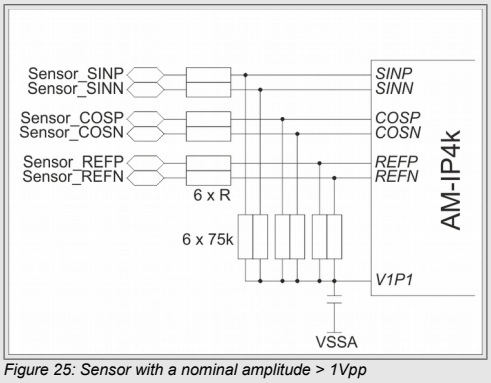


Figure 25: Sensor with a nominal amplitude > 1Vpp

- The nominal amplitude of the AM-IP4k is set to 500mVpp by the configuration bits `GAIN(1:0)`.
- The reference level `V1P1` is generated **internally**.
- Resistors between the input signals and `V1P1` are used as voltage divider. The resistor value R is calculated as follows: R = (V_{SENSOR} / 500mV - 1)x75 kΩ
- Sensor amplitude as well as the sensor's mean voltage are divided in a ratio of (75kΩ+R)/75kΩ.

Sensor with single-ended output signals (I)

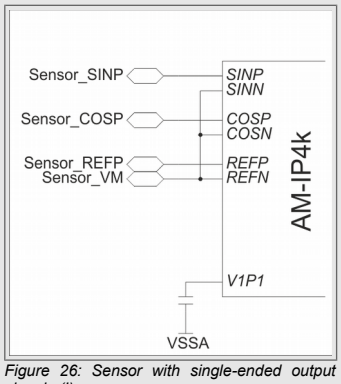


Figure 26: Sensor with single-ended output signals (I)

- The sensor amplitude and the nominal amplitude of the AM-IP4k are harmonised by the configuration bits `GAIN(1:0)`.
- The reference level `V1P1` is provided **by the sensor**.

Sensor with single-ended output signals (II)

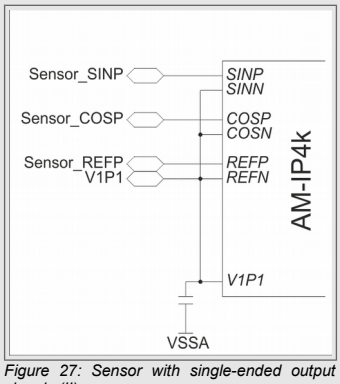


Figure 27: Sensor with single-ended output signals (II)

- The sensor amplitude and the nominal amplitude of the AM-IP4k are harmonised by the configuration bits `GAIN(1:0)`.
- The reference level `V1P1` is generated **internally** and made available to the sensor.

Sensor with antiparallel photodiodes
Adjustment of amplitude equality possible

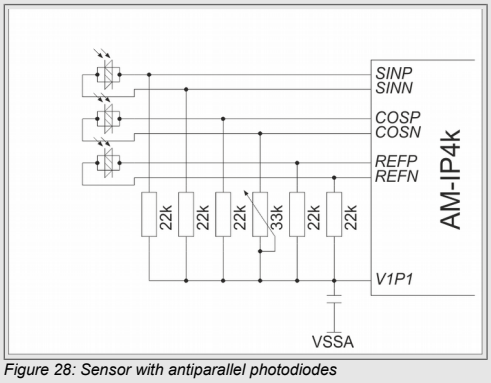


Figure 28: Sensor with antiparallel photodiodes

- The nominal amplitude of the AM-IP4k is set to 500mVpp by the configuration bits `GAIN(1:0)`.
- The reference level `V1P1` is generated **internally**.
- By modifying the cosine signal's amplitude amplitude equality is adjusted. The test signals `SMON` and `CMON` are used for the adjustment.
- Resistors between the input signals and `V1P1` are used as current-to-voltage converters. The resistor value R is calculated as follows: R = 500mV / (2·I_{SENSOR}) and $P_{AMPL} \approx 1.5 \cdot R_{FIX}$
  → In this example: $I_{SENSOR} = 11\ \mu A_{pp}$

Photodiode array with joint cathode or anode
Adjustment of amplitude equality and offset possible

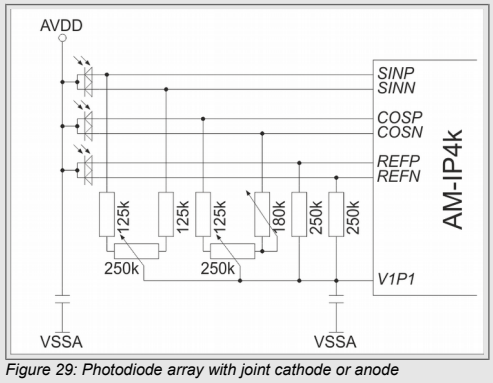


Figure 29: Photodiode array with joint cathode or anode

- The nominal amplitude of the AM-IP4k is set to 250mVpp by the configuration bits `GAIN(1:0)`.
- The reference level `V1P1` is generated **internally**.
- By modifying the cosine signal's amplitude amplitude equality is adjusted. Then, the offset for both signals can be adjusted using the test signals `SMON` and `CMON`.
- Resistors between the input signals and `V1P1` are used as current-to-voltage converters. The resistor value R is calculated as follows: R = 250mV / (2·I_{SENSOR}). This resistor is partly designed as a potentiometer for offset adjustment: $P_{OFFS} \approx R$; $R_{FIX} \approx ½\ R$; $P_{AMPL} \approx 1.5 \cdot R_{FIX}$
  → In this example: $I_{SENSOR} = 0.5\ \mu A_{pp}$

Sensor for current signals 11 µApp

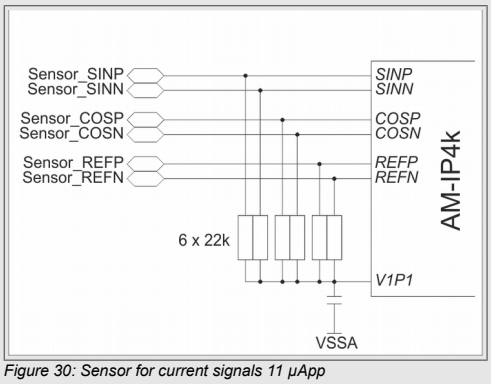


Figure 30: Sensor for current signals 11 µApp

- The nominal amplitude of the AM-IP4k is set to 500mVpp by the configuration bits `GAIN(1:0)`.
- The reference level `V1P1` is generated **internally**.
- Resistors between the input signals and `V1P1` are used as current-to-voltage converters. The resistor value R is calculated as follows: R = 500mV / (2·I_{SENSOR})
  → In this example: $I_{SENSOR} = 11\ \mu A_{pp}$

11.3 EEPROM

The EEPROM is accessed by an internal interface, controlled by `EEP` register accesses:

- The bit `EEPBSY` has to be set to ‘0’ before every write-access.
- Write-accesses to `EEPOPC` (Byte 3) trigger an EEPROM activity. `EEPADR` and if necessary `EEPDAT` must be valid.
- Invalid OP codes must not be used.

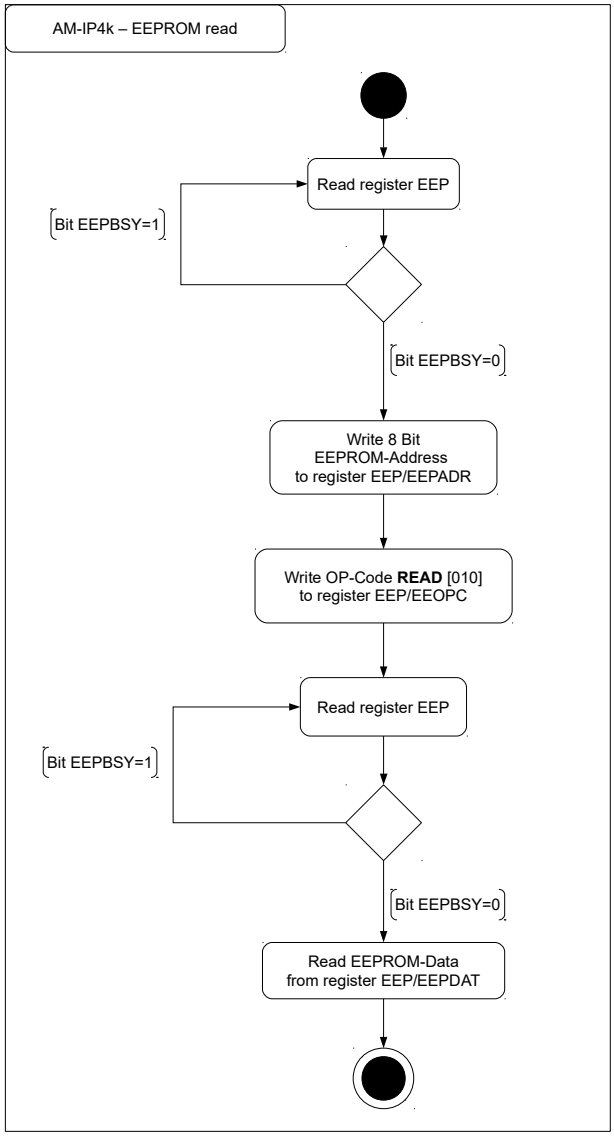


Figure 31: Procedure sequence for EEPROM read

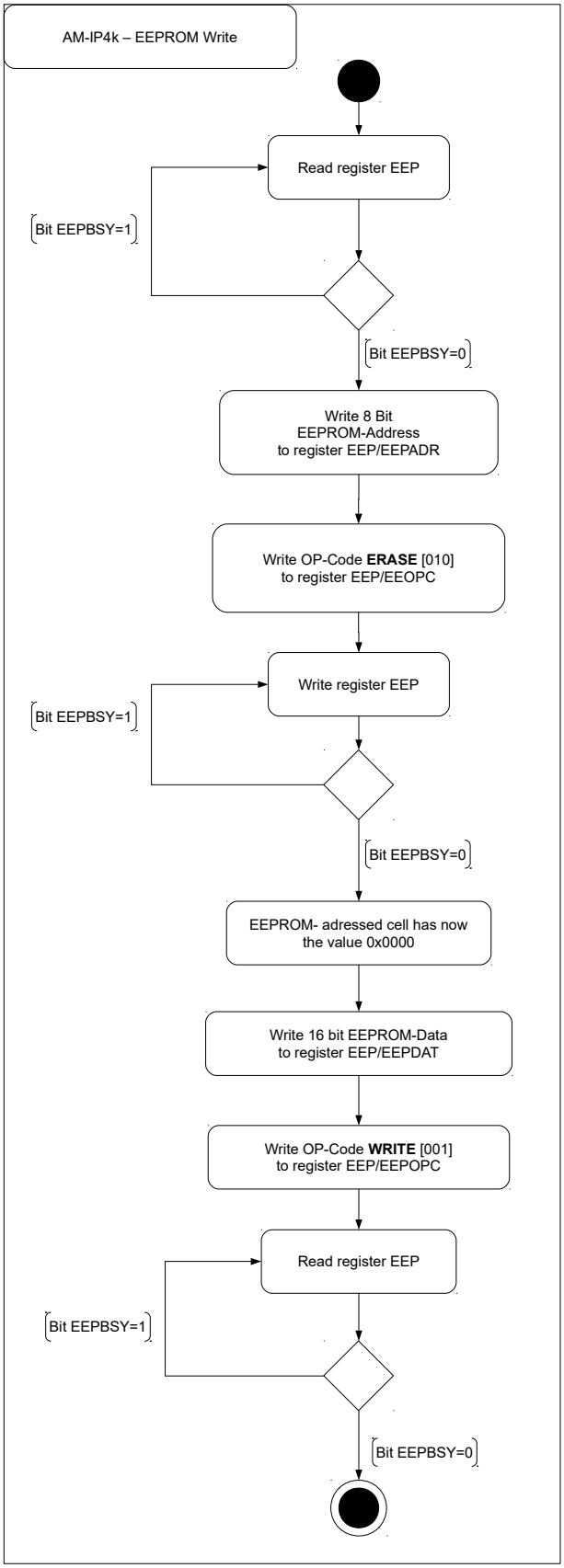


Figure 32: Procedure sequence for EEPROM read

Notes