Level shifter GC-LS

Datasheet

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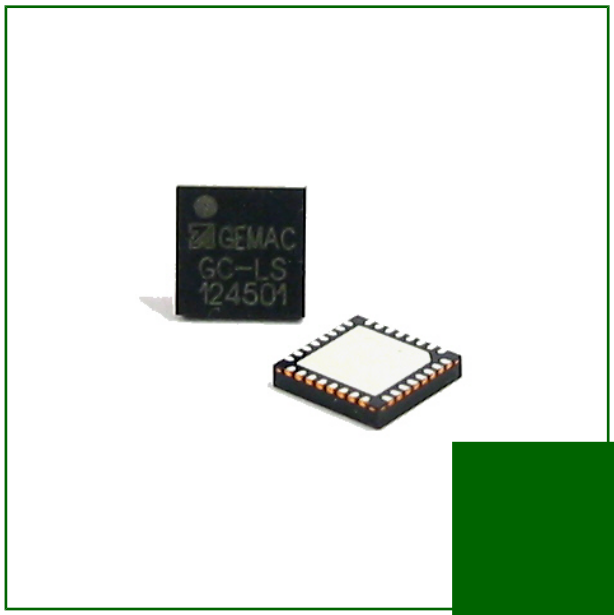

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Revision Overview

Date	Revision	Change(s)
20.03.2013	1.0	First version, preliminary version
19.06.2013	1.1	completed
31/03/2017	1.2	change to new AMAC document layout

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1. Overview

The four-channel level shifter circuit *GC-LS* is used for adjusting the voltage level between 5V encoders for distance or angle measurement and interpolation circuits with 3.3V operating voltage. Typically, standardized encoders and measuring bridges use a supply voltage of 5V and a common mode voltage of 2.5V. To connect these encoders with systems of 3.3V power supply, the conversion of the common mode voltage and amplitude is possible by using the *GC-LS.* Apart from the conversion of differential signals to differential ones also the conversion of single ended signals to differential signals can be performed. Due to its four channels, the IC is suited for incremental measurement systems with reference track or two-track systems. The input stage of the IC is realized by an instrumentation amplifier with high impedance inputs. Thus, the measurement signals are transferred unadulterated to the outputs, also these of high-impedance measuring bridges. Additionally, a 5V to 3.3V line regulator is implemented for supplying circuits with 3.3V operating voltage, e.g. controllers, *GC-NIP, GC-IP201 (B).*

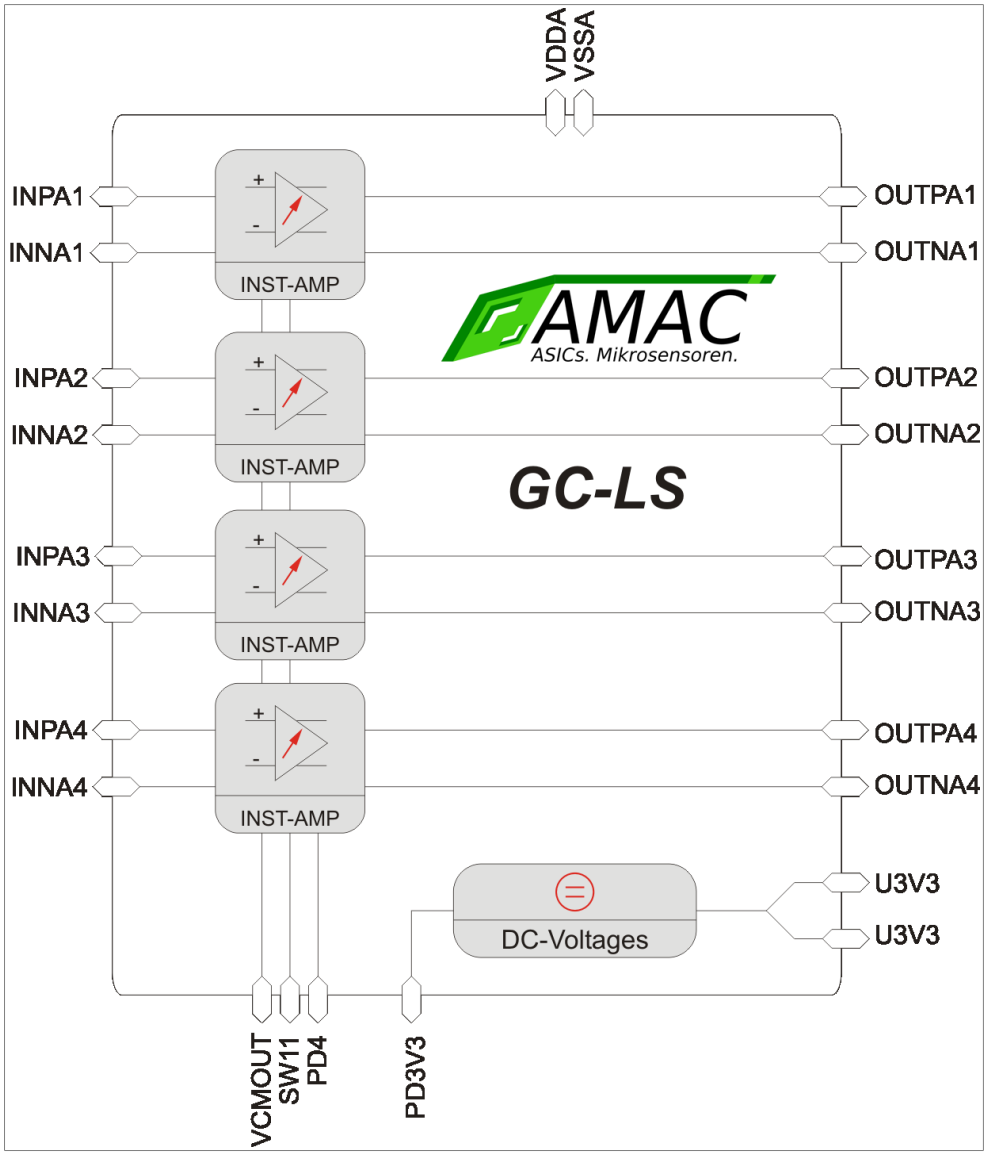

Figure 1: Blockschaltbild

2. Features

- Adjustment of voltage level between 5V encoders for distance or angle measurement and interpolation circuits with 3.3V operating voltage
- integrated 3.3V voltage regulator for external circuit, linear controller can be switched off
- four channels
- differential or single-ended inputs
- high input impedance
- differential outputs
- 1,5 MHz cut-off frequency
- amplification 0 or -3,5dB; adjustable
- channel 4 can be switched off
- available as bare die or in QFN 32 (5x5x0,8 mm)

3. Description of Functions

The IC contains four level shifters with differential inputs and differential outputs. Encoders with voltage interface and measuring bridges can be directly connected at the inputs. The common mode voltage of the inputs is typically set to VDDA/2, the common mode voltage of the outputs is set to the voltage value at pin VCMOUT. The level shifters are designed for the conversion of single ended and differential input signals. According the adjusted amplitude, the output signals are available differentially. In addition, a 5V to 3.3V line regulator is implemented to be used for power supply of other components. To optimize the power consumption, unneeded functional blocks of the IC can be set into power-down mode.

Table 1: Configuration output level

PIN SW11	Common mode voltage	Differential amplitude	Application example
0 (Low)	Voltage at Pin VCMOUT	0.66 x Differential voltage (INP-INN)	$1V_{pp}$ – sensor
1 (High)	Voltage at Pin VCMOUT	1.00 x Differential voltage (INP-INN)	bridge sensor, conversion single-ended signals to differential

Table 2: Configuration channel 4

PIN PD4	Channel 4	Application examples
0 (Low)	enabled	2-track-vernier, 2-channel incremental encoders without reference track
1 (High)	in power-down	1-channel incremental system with reference track

Table 3: Configuration voltage controller

PIN PD3V3	Voltage regulator 3,3V	Application examples
0 (Low)	enabled	System consisting of sensor, *GC-LS* and interpolation circuit (e.g. *GC-NIP, GC-IP201(B)*)
1 (High)	in power-down	System with own power supply 3,3V

4. Parameters

Table 4: Absolute maximum ratings

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
VDDA	Analogue supply voltage	-0.5		7,0 [1)]	V
TJ	Operating temperature	-40		125	°C
TS	Storage temperature	-55		150	°C
V(AIN)	Voltage at the analogue inputs	-0.3		VDDA+0.3	V
V(DIN)	Voltage at the configuration inputs	-0.3		VDDA+0.3	V
ESD	ESD-sensitivity (HBM)			2	kV

[1)] t < 250ms, T < 60°C

Table 5: Operating conditions

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
VDDA	Analogue supply voltage	4,5	5V	5,5	V
I(VDDA)	Power consumption		2		mA
T	Operating temperature	-40		125	°C

Table 6: Characteristic values

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
Z(AIN)	Input impedance		1GΩ||8pF		
Gain	Gain according 1 @1kHz	98	100	102	%
fg	Cut-off frequency (-3dB)		1,5		MHz
CMIR	Common mode input voltage @(V_{IN} < 1,0V_{pp}, Offset = 0V)	0,85	2,5	VDDA-1,5	V
CMRR	Common mode rejection (@ f < 1kHz, `SW11=1`)	45			dB
V(VCMOUT)	Common mode output voltage @(V_{IN} < 1,5V_{pp}, , `SW11=0`)	0,75	1,5	VDDA-1,0	V
V(VCMOUT)_SW11	Common mode output voltage @(V_{IN} < 1,5V_{pp}, , `SW11=0`)	0,75	2,5	VDDA-1,0	V
I(OUTX)	Output current at Pin `OUTPx/OUTNx`			0,5	mA
CL(OUTX)	Capacitive load at Pin `OUTPx/OUTNx` @fg-1db 800kHz			100	pF
CL(OUTX)	Capacitive load at Pin `OUTPx/OUTNx` @fg-1db 200kHz			1000	pF
V(U3V3)	Output Voltage, Pins `U3V3`	3,2	3,3	3,4	V
I(U3V3)	Total current at Pins `U3V3`			50	mA
ΔV(U3V3)	Load regulation, Pins `U3V3@I(U3V3)` ≤ 50mA			35	mV
CL(U3V3)	Capacitive load at Pins `U3V3`	10			µF
VIH	Input voltage High at Pin `SW11/PD4/PD3V3`	0,6*VDDA		VDDA	V
VIL	Input voltage Low at Pin `SW11/PD4/PD3V3`			0,2*VDDA	V

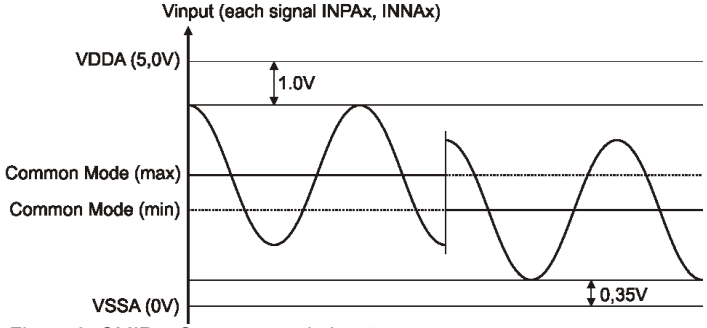

Figure 2: CMIR – Common mode input range

5. Package / Die

5.1. QFN 32

QFN 32 (5x5), Pitch 0,5

Table 7: QFN32 Pin-list

Pin QFN32	Name	Type	Description	Comment
1	OUTPA4	Analogue output	Output 4 - non inverting output	Differential output – channel 4
2	OUTNA4	Analogue output	Output 4 - inverting output	Differential output – channel 4
3	OUTPA3	Analogue output	Output 3 - non inverting output	Differential output – channel 3
4	OUTNA3	Analogue output	Output 3 - inverting output	Differential output – channel 3
5	OUTPA2	Analogue output	Output 2 - non inverting output	Differential output – channel 2
6	OUTNA2	Analogue output	Output 2 - inverting output	Differential output – channel 2
7	OUTPA1	Analogue output	Output 1 - non inverting output	Differential output – channel 1
8	OUTNA1	Analogue output	Output 1 - inverting output	Differential output – channel 1
9	n.c.		n.c.	-
10	U3V3	Power output	Voltage regulator +3,3V	internal connected with Pin 11 Power supply for further external components 3,3V
11	U3V3	Power output	Voltage regulator +3,3V	internal connected with Pin 10 Power supply for further external components 3,3V
12	VDDA	Power	Supply voltage +5,0V	Power supply
13	VDDA	Power	Supply voltage +5,0V	Power supply
14	n.c.		n.c.	-
15	PD3V3	Digital input Pull Down	Disable 3,3V-voltage regulator	L: 3,3V-voltage regulator enabled; H: 3,3V-voltage regulator in power-down
16	n.c.		n.c.	-
17	VSSA	Power	Supply voltage 0V	Power supply ground
18	PD4	Input digital Pull Down	Power Down of channel 4	L: channel 4 enabled H: channel 4 in Power-Down
19	INNA1	Analogue input	Input 1 - inverting	Differential input channel 1[1)]
20	INPA1	Analogue input	Input 1 - non inverting	Differential input channel 1
21	INNA2	Analogue input	Input 2 - inverting	Differential input channel 2[1)]
22	INPA2	Analogue input	Input 2 - non inverting	Differential input channel 2
23	INNA3	Analogue input	Input 3 - inverting	Differential input channel 3[1)]
24	INPA3	Analogue input	Input 3 - non inverting	Differential input channel 3
25	INNA4	Analogue input	Input 4 - inverting	Differential input channel 4[1)]
26	INPA4	Analogue input	Input 4 - non inverting	Differential input channel 4
27	n.c.		n.c.	-
28	VSSA	Power	Supply voltage 0V	Power supply ground
29	VCMOUT	Analogue input	Common Mode Output Voltage	Reference level of output signals
30	VDDA	Power	Supply voltage +5,0V	5V Power supply
31	SW11	Input digital Pull Down	Configuration gain factor	L: gain 0,66 H: gain 1,0
32	n.c.		n.c.	-
EP	VSSA	Package	Ground 0V	Exposed Pad

[1)] *2.5V (half of the sensor output voltage range) has to be applied if single ended input signals are used.*

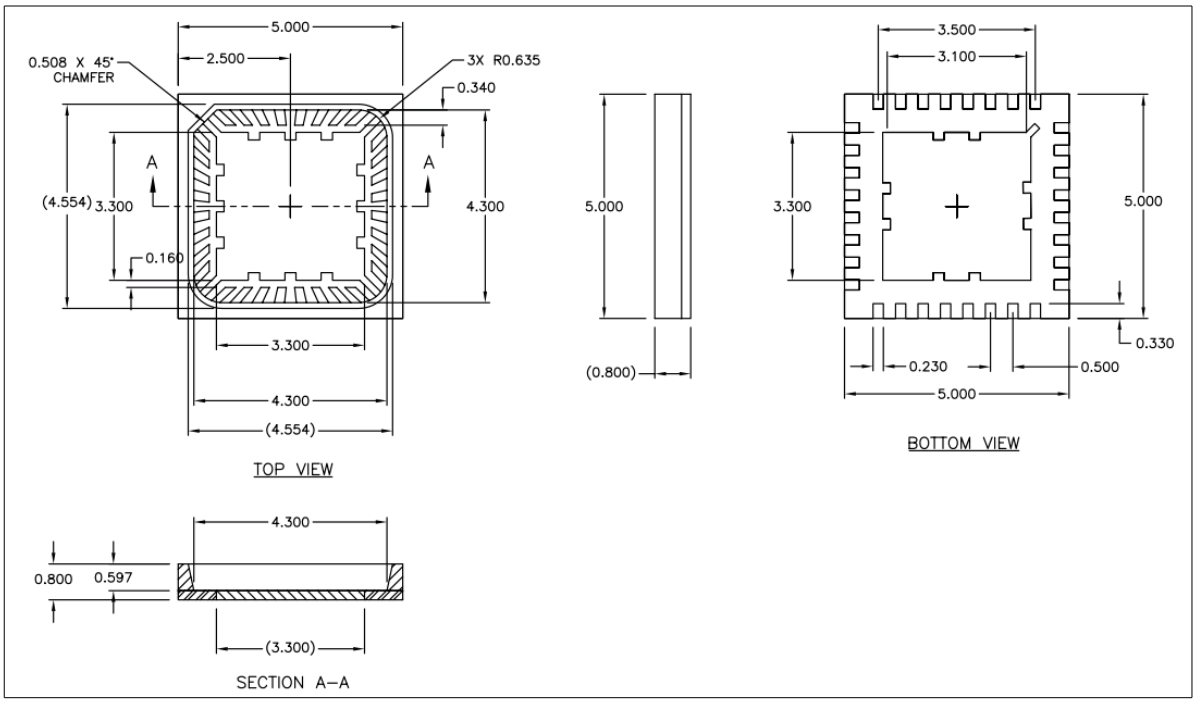

Figure 3: Package QFN32

5.2. Die – Pad coordinates

The following table shows the coordinates of the 27 pads of the die. The coordinates refer to the centre of the bond pad. The origin of coordinates is the lower left corner of the die

Pad size: 85µm x 85µm
Chip size: 1,580µm x 2,565µm

Table 8: Pad coordinates

X_Centre (µm)	Y_ Centre (µm)	Name
49,5	335,4	INPA4
49,5	545,4	INNA4
49,5	755,4	INPA3
49,5	965,3	INNA3
49,5	1175,3	INPA2
49,5	1385,3	INNA2
49,5	1595,3	INPA1
49,5	1805,1	INNA1
49,5	1964,9	PDA4
49,5	2085,35	VSSA
49,5	2195,35	PD3V3
538,05	2419,7	VDDA
762,6	92,5	VCMOUT
519,25	92,5	VSSA

X_Centre (µm)	Y_ Centre (µm)	Name
751,15	2419,7	VDDA
994,5	2419,7	U3V3
1482,6	2123,15	U3V3
1482,6	1743,1	OUTNA1
1482,6	1613,1	OUTPA1
1482,6	1353,1	OUTNA2
1482,6	1223,3	OUTPA2
1482,6	963,5	OUTNA3
1482,6	833,5	OUTPA3
1482,6	573,5	OUTNA4
1482,6	443,5	OUTPA4
1482,6	333,5	SW11
1003,55	92,5	VDDA

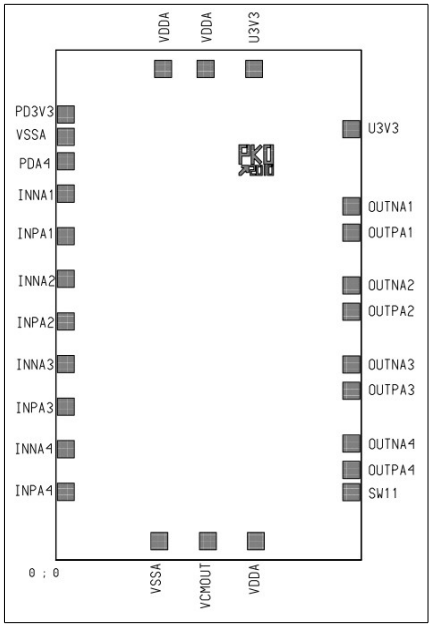

Figure 4: GC-LS Die

6. Application instructions

6.1. Board design

The GC-LS has been primarily designed for conditioning of sensor signals for connection to an interpolation circuit, for example GC-IP201(B). Therefore, the same design rules as for the use of A/D converters shall be applied. It should be noted that the quality of the power supply for standard sensors affect the measurement accuracy. If necessary, additional LC combinations for sensor power supply and for VDDA have to be used. Therefore, the supply voltage, the reference voltage and the 3.3V voltage controller output have to be wired at least according to the recommendations in table 9 and for unused inputs / outputs according to table 10.

Table 9: external components

Pin	Components / design hints
VSSA	should be designed at PCB as area
VDDA	Power supply 5,0V one block capacitor of 100nF per VDDA port to VSSA (optional 100pF parallel) additionally one common block capacitor of 10µF for all VDDA pins to VSSA area
VCMOUT	block capacitor of 100nF to VSSA (optional 2,2µF parallel)
U3V3	block capacitor of 10uF to VSSA

Table 10: unused inputs and outputs

Pin	if unused
INPAx / INNAx	≈2.5V have to be applied
INPA4 / INNA4	Can be left open if PDA4 = High, otherwise 2.5V have to be applied
PD4	internal pull-down resistor* (channel4 active – default)
SW11	internal pull-down resistor* (amplification = 0,66 - default)
U3V3	can be left open if unused (PD3V3 = High), otherwise capacitor of 10 µF to VSSA
PD3V3	internal pull-down resistor* (voltage regulator active - default)

** The internal pull-up resistors prevent unpredictable behaviour of the IC, caused by open inputs. For reliable operation, all inputs must be wired as defined.*

Furthermore:

- All block capacitors shall be arranged close to the pins.
- A ground plane for VSSA shall be provided.
- For a reliable operation, all inputs must be wired as defined. At the pins PD4, SW11 and PD3V3, the additional connection of an external pull-down resistance (10k) is recommended.
- For additional terminating resistors between INPAx and INNAx, refer to the application instructions of the respective sensor manufacturer.
- Single-ended sensors are usually connected to the inputs INPAx. For this, the DC reference levels of the IC (INNAx) and the sensor must match.
- The connections shall be short and of low capacitance.

The following figure shows an application example. The signals of a 5V full bridge sensor (differential) shall be converted for post-processing by operating circuits with 3.3V supply e.g. GC-NIP, GC-IP201 (B) or controllers.

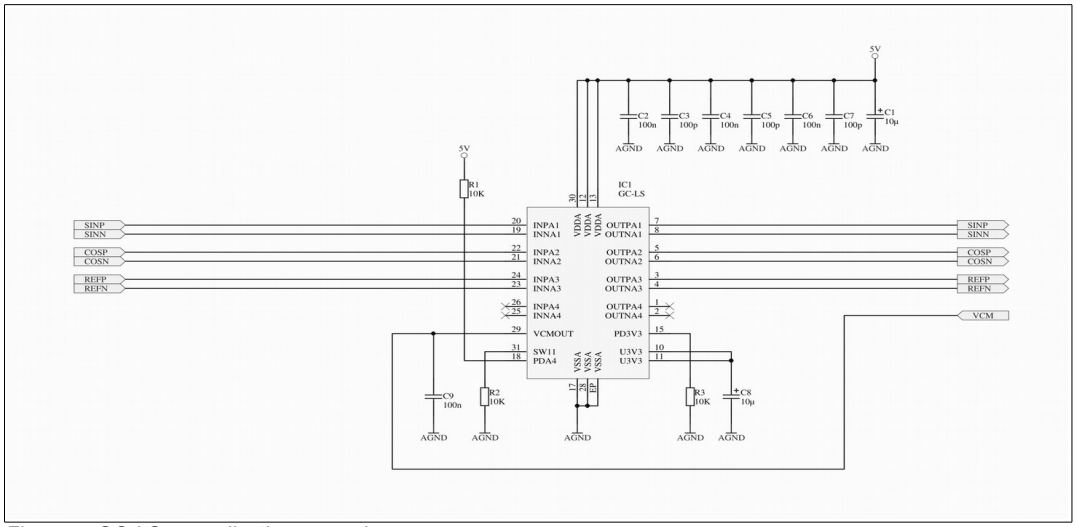

Figure 5: GC-LS – application example

7. Ordering information

Product type	Description/differentiation	Article number
GC-LS Die	4 channel analogue level shifter 5V to 3,3V, Die	PR-44500-01
GC-LS	4 channel analogue level shifter 5V to 3,3V, QFN32 (5x5)	PR-44500-00

8. Notes