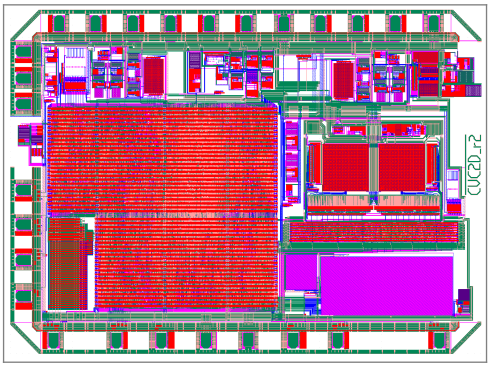
AM-CVC2D

Datasheet

Version: 0.1
Datum: 15/04/2021



AMAC ASIC- und Mikrosensoranwendung Chemnitz GmbH
Kopernikusstr. 16
D-09117 Chemnitz
Germany

Tel.: +49 371 334204 - 0
Fax: +49 371 334204 - 69
E-Mail: info@amac-chemnitz.de
Web: www.amac-chemnitz.de

Revision history

Date	Revision	Changes
30/01/2020	0.1	First version

Table of contents

1 Overview 6
2 Specifications 7
3 Ordering information 7
4 Pin assignment 8
5 Package / Die 9
5.1 Pin configurations 9
5.2 Package drawing CLDCCJ28 (Chip) 9
6 Functional description 10
6.1 Reference voltage 10
6.2 DAC / Driver 10
6.3 Charge amplifiers (X_CHAMP, Y_CHAMP) 11
6.4 Amplifier (XY_AMP) 11
6.5 ADC 12
6.6 Temperature sensor (VTEMP) with ADC 12
6.7 Clock generator (CLOCK) 12
6.8 Sensor control 12
6.8.1 Timing sensor excitation / normal mode 14
6.9 Digital signal processing 17
6.9.1 Sensor signal correction 17
6.9.2 FIR-Filter 18
6.9.3 Threshold detection 18
6.9.4 Real-time data transmission 19
6.10 SIL block 21
7 Interfaces 22
7.1 SPI-Interface 22
7.1.1 SPI signals 22
7.1.2 SPI protocol 22
7.1.3 Register access 23
7.1.4 SRAM and EEPROM access 23
7.1.5 SPI specifications 24
7.2 I^2C-Interface 25
7.2.1 I^2C signals 25
7.2.2 I2C protocol 25
7.2.3 Register access 26
7.2.4 EEPROM/SRAM access 26
8 Register and internal memory 28
8.1 Configuration registers 28
8.2 Data registers 29
8.3 SRAM – Buffer for FIR filter coefficients 29
8.4 EEPROM content 30
8.5 Configuration registers description 31
8.5.1 Clock configuration / Operating modes registers 31
8.5.2 Sensor control registers 32
8.5.3 Sensor monitoring / SIL registers 33
8.5.4 Sensor signal correction and evaluation registers 34
8.5.5 Test-/Special registers 35
9 Contact 36

List of figures

Figure 1: AM-CVC2D Block diagram....6
Figure 2: Pin configuration AM-CVC2D....9
Figure 3: Package technical drawing CLDCCJ28....9
Figure 4: Timing sensor excitation (1-channel, single-ended sampling)....14
Figure 5: Sensor excitation power on cycle....14
Figure 6: Timing sensor excitation (1-channel, dual single-ended sampling)....15
Figure 7: Timing sensor excitation (2-channel, single-ended sampling)....15
Figure 8: Timing sensor excitation (2-channels, dual single-ended sampling), part 1....16
Figure 9: Timing sensor excitation (2-channel, dual single-ended sampling), part 2....16
Figure 10: Block diagram digital signal processing....17
Figure 11: Block diagram sensor signal correction....17
Figure 12: SPI master 24 bit transmission....19
Figure 13: SPI master 3 x 8 bit transmission....20
Figure 14: I^2C real time data read 3 x 8 *bit transmission*....20
Figure 15: SIL block for self-testing / intrinsic safety diagram....21
Figure 16: SPI transmission format....22
Figure 17: I^2C register write 1....26
Figure 18: I^2C register write 2....26
Figure 19: I^2C register read....26
Figure 20: I^2C EEPROM/SRAM write....26
Figure 21: I^2C EEPROM/SRAM read....27

List of tables

Table 1: General technical specifications....7
Table 2: Pin description....8
Table 3: Parameter reference voltage....10
Table 4: DAC parameters....10
Table 5: Driver parameters....10
Table 6: Detuning examples for VXPEP....11
Table 7: Charge amplifiers parameters....11
Table 8: Parameter output amplifier....12
Table 9: Temperature sensor parameters....12
Table 10: Clock generator parameters....12
Table 11: Sensor clock division per sampling mode....13
Table 12: Maximum adjustable sensor frequency as per mode....13
Table 13 FIR-Filter configuration at XENA_FIR and YENA_FIR....18
Table 14 Threshold detection flags and reference values....18
Table 15*: Data select SENDREG*....19
Table 16: Real-time data transmission, data at MOSI/MISO....20
Table 17: SPI signals....22
Table 18: SPI protocol, MOSI data....22
Table 19: SPI protocol, MISO data....23
Table 20: SPI protocol, designation....23
Table 21: Sequence register write access....23
Table 22: Sequence register read access....23
Table 23: EEPROM/SRAM access select....23
Table 24: Sequence: RAMRWSPI....24
Table 25: Sequence EEPROM/SRAM write access....24
Table 26: Sequence EEPROM/SRAM read access....24
Table 27: SPI timing and electrical specifications....24
Table 28: I^2C signals....25
Table 29: I2C slave address configuration....25
Table 30: I2C OP codes....25
Table 31: Format meaning....25
Table 32: I^2C SDA data....27
Table 33: Configuration registers assignment....28
Table 34: Data registers assignment....29
Table 35: SRAM: FIR coefficients buffer....29
Table 36: EEPROM: configuration registers and SRAM....30
Table 37: Clock configuration and operating modes registers....31
Table 38: Sensor control registers....32
Table 39: Sensor monitoring / SIL registers....33
Table 40: Sensor signal correction and evaluation registers....34
Table 41: Test-/Special registers....35

1 Overview

The AM-CVC2D is a two-channel charge amplifier with analogue and digital outputs, fully configurable. The IC serves for sensor excitation and charge evaluation. The IC uses as charge input two external capacitive sensors and can be controlled via a serial protocol. The AM-CVC2D consists of a mixed-signal integrated circuit, which is composed of the following components:

- Sensor controlling/optimization.
- 10 bit DAC for adjustment of the excitation voltages.
- Driver for generation of the recharging voltages for continuous and self-test modes.
- Internal reference voltage via adjustable band gap
- Two charge amplifiers with programmable offset and integration capacitances
- Two sample-and-hold amplifiers for the analogue outputs
- Amplifier for analogue signal before the A/D converter
- 14 bit A/D converter of the analogue signals
- Digital sensor characteristic curves and temperature correction
- FIR filter block of four filters, with up to 31 selectable sampling points per filter
- Digital configuration of threshold detection
- Component for handling SIL-relevant measurements and test cases (self-test after Power-ON, continuous test of two counter phase sensor elements of the same axis)
- Analogue multiplexer for output of analogue voltage, test, or reference voltage
- SPI and I²C Interface
- Real-time data transmission from ASIC, SPI master mode
- Power-On-Reset (POR) with configuration from EEPROM
- Internal clock generator
- Internal temperature sensor

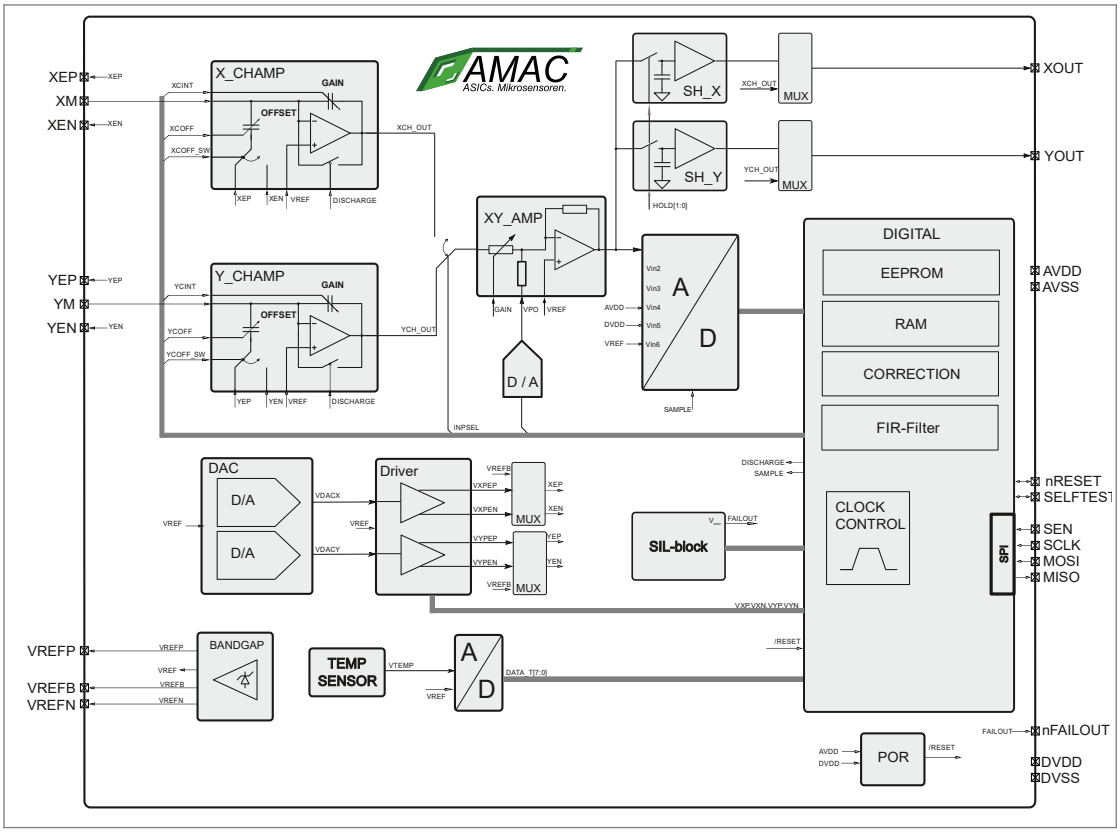


Figure 1: AM-CVC2D Block diagram

2 Specifications

Table 1: General technical specifications

Parameter	Characteristic value
Operating voltage:	3.3V, ±5% (DVDD / AVDD)
Current consumption:	≤ 15mA
Operating temperature range:	-40 … +150°C
Clock:	Internal RC oscillator set to a nominal frequency of 40 MHz Configurable carrier frequency
Reference voltage: (VREF)	Can be set in 16 steps each of 8 mV (4 bit), nominal 1.2 V
Power On Reset:	Resetting of all registers Loading of configuration from the integrated EEPROM Start time, including EEPROM read-out at 150 KHz: nominal 10.5 ms
Driver for sensor excitation:	Generation of the recharging voltages XEP/XEN and YEP/YEN Voltages are configured symmetrically to VREF = 1.2 V Setting range: 0 V_{PP}…± 1.5 V_{PP} in 0.146mV steps (10 Bit)
Charge amplifier: X_CHAMP, Y_CHAMP	Built-in configurable integration capacitance Setting range: 0.0 pF – 12.8 pF in 100 fF steps Tolerance $C_{internal}$ ±20%, C_{total} <100 pF ($C_{internal}$ + C_{sensor}) Offset compensation for sensor; ΔC_{MAX}: ± 3.2 pF in 25 fF steps Sensor's parallel resistor R_{ISO} > 20MΩ

3 Ordering information

Product type	Description	Article number
AM-CVC2D	Capacitance to voltage converter, two channel, digital output	PR-51600-00

This integrated circuit can be damaged by ESD. AMAC recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4 Pin assignment

Table 2: Pin description

Pin Nr. CLDCCJ28 Single-Chip	Name	Type	Description
1	VDDA	AP	Analogue voltage supply
2	XE1	AO	X-channel, XE1 excitation voltage output
3	XM	AI	X-channel, charge amplifier input
4	XE2	AO	X-channel, XE2 excitation voltage output
5	VSSA	AP	GND, analogue
6	VCM	AO	Buffered reference voltage
7	VREFH	AO	Buffered reference voltage
8	YE2	AO	Y-channel, YE2 excitation voltage output
9	YM	AI	Y-channel, input charge amplifier
10	YE1	AO	Y-channel, YE1 excitation voltage output
11	VREFL	AO	Buffered reference voltage
12	XYCH_OUT	AO	XY-channel, test pin sensor output voltage
13	ADDR0	DI	I2C slave address select
14	ADDR1	DI	I2C slave address select
15	IFC_SEL	DI (PU)	Interface select (1= SPI, 0= I^2C)
16	NRES	DIO (PU)	Reset and Stand-By, L-active (I=ext. Reset; O=Status internal POR)
17	SEN	DI	SPI (Slave mode), Chip-Select, L-active I^2C: Clock
18	nFAILOUT	DOD	Error, Open-Drain, L-active Sensor test, supply power, or Temperature not OK or a threshold flag is active
19	nCS_MA	AO	SPI (Master mode): Chip select, low active
20	SCK_MA	DI	SPI (Slave mode), clock input SPI(Master mode), clock output
21	BUSY	DO	Busy
22	VDD	DP	Digital voltage supply
23	VSS	DP	GND, digital
24	MISO	DOS	SPI, Data output + Busy + Status internal POR
25	MOSI	DIO	SPI (slave mode), Data input SPI (master mode), Data output I^2C: data
26	CLK	DI	External CLOCK input

AP = Analogue power supply,
DP = Digital power supply,
AI = Analogue input, AO = Analogue output,
DI = Digital Input, DO = Digital Output, DOD = Digital Output ; Open Drain,
DIO = Digital input and output,
DOS = Digital output, active tristate, PU = Internal pull-up, PD = Internal pull-down

5 Package / Die

5.1 Pin configurations

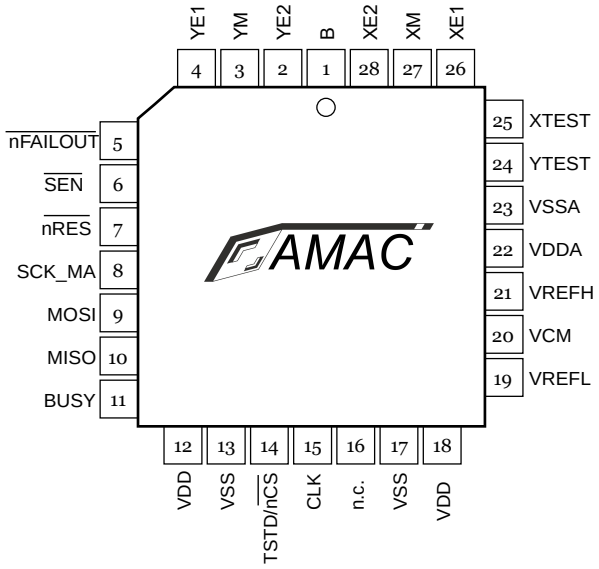


Figure 2: Pin configuration AM-CVC2D

5.2 Package drawing CLDCCJ28 (Chip)

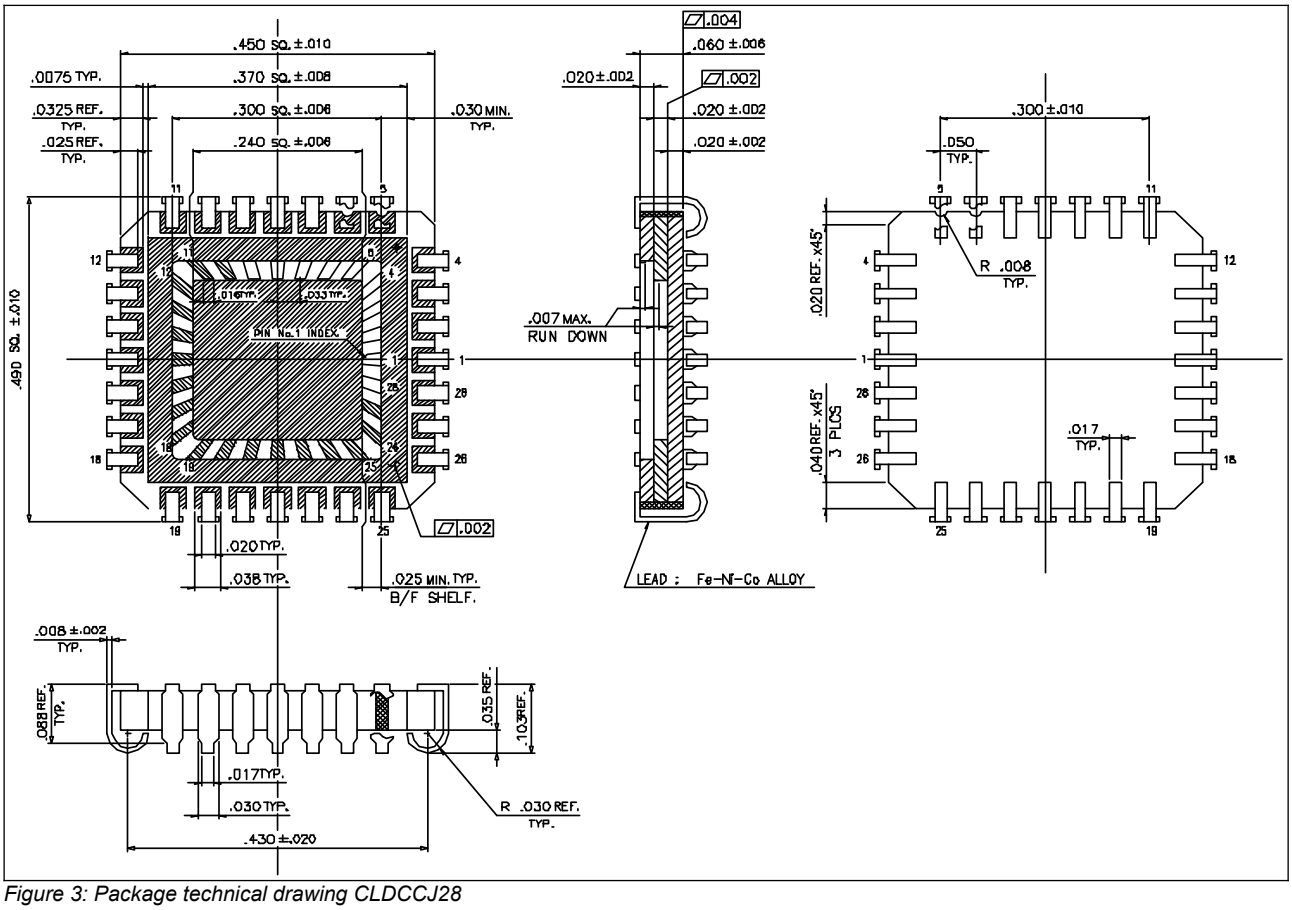


Figure 3: Package technical drawing CLDCCJ28

6 Functional description

6.1 Reference voltage

- Source of the internal reference voltages REFM, REFH, REFL

Table 3: Parameter reference voltage

Parameter	Min.	Nom.	Max.	Unit
Mean reference voltage REFM* (Charge amplifier)	TBD.	1.2	TBD.	V
High reference voltage REFH (ADC)		1.8		V
Low reference voltage REFL (ADC)		0.6		V
Increment for VREFB adjustment (4Bit)		8		mV
Offset voltage OPV buffered VREFB	-10		+10	mV
Accuracy as function of temperature, at AVDD = 3.3V	-150		+200	ppm·K^{-1}

*Adjustment is performed by the manufacturer

6.2 DAC / Driver

- D/A converter with a 10 bit resolution for the supply of the programmable voltages
- VXP, VXN, VYP, and VYN are the amplitude settings for the sensor excitation voltage.
- XPHASE, YPHASE carry the phase information.
- Generation of the recharging voltages XEP/XEN and YEP/YEN for sensor excitation from VXPEP/VXPEN and VYPEP/VYPEN correspondingly.

The VXP, VXN, VYP, and VYN are 10 bit long registers with a range from 0 to 1023 which is seen as the (2*VREF … 0) See 8.5.2.

Table 4: DAC parameters

Parameter	Min.	Nom.	Max.	Unit
Reference voltage VREF		1.20		mV
DAC increment		1.173		mV
Non-linearity (± 3σ STW)		TBD		INC

Table 5: Driver parameters

Parameter	Min.	Nom.	Max.	Unit
Setting range for: XEP, YEP, XEN, and YEN	0		2*VREF	mV
Center voltage between XEP and XEN or YEP and YEN		VREF		
Total of the max. load capacitance at the driver's output to ground or XM/YM			TBD	pF

The DAC multiplexer works with one input value at a time, done with an internal select. So the DAC values are selected between VXPEP, VXPEN, VYPEP, and VYPEN.

Additionally it also takes into account the resulting detuning value of the mentioned voltages, when the self test mode is activated, via ST_MODE = 1. The detuning voltage is set with the register VXPED and VYPED. See example for VXPEP, table 6. Same applies for VXPEN, VYPEP, and VYPEN.

$$VXPEP_{Detunning} = VXPEP \pm VXPED(5:0) \quad [1]$$

Table 6: Detuning examples for VXPEP

Parameter	detuning direction bit	Detuning bits(5:0)	Resulting detuning
VXPEP	VXPED(6)=0 VXPED(6)=1	VXPED(5:0)= 00_0000	VXPEP
	VXPED(6)=0 VXPED(6)=1	VXPED(5:0)= 00_0001	VXPEP - 8 VXPEP + 8
	VXPED(6)=0 VXPED(6)=1	VXPED(5:0)= 00_0010	VXPEP - 16 VXPEP + 16
	VXPED(6)=0 VXPED(6)=1	VXPED(5:0)= 01_1111	VXPEP - 248 VXPEP + 248
	VXPED(6)=0 VXPED(6)=1	VXPED(5:0)= 11_1111	VXPEP - 504 VXPEP + 504

6.3 Charge amplifiers (X_CHAMP, Y_CHAMP)

- Charge amplifiers with programmable offset and integration capacitances

The integration capacitance values can be set at the sensor control registers `XCINT` and `YCINT` for each channel. Also at `XCOFF` and `YCOFF` registers for the offset capacitance values.

For the integration capacitances the range value goes from 0 to 12.7 pF and is incremented in 0.1 pF steps. And for the offset capacitances the range value goes from 0 to 3.175 pF and is incremented in 0.025 pF steps.

Table 7: Charge amplifiers parameters

Parameter	Min.	Nom.	Max.	Unit
Minimum integration capacitance		0.0		pF
Maximum integration capacitance		12.7		pF
Resolution integration capacitance		100		fF
Tolerance integration capacitance	-20		20	%
Minimum offset capacitance		0.0		pF
Maximum offset capacitance		3.175		pF
Resolution offset capacitance		50		fF
Tolerance offset capacitance	TBD		TBD	%
Matching error between X and Y channels	TBD		TBD	%
Input offset	TBD		TBD	mV
Output voltage range	TBD		TBD	V

6.4 Amplifier (XY_AMP)

- Offset correction of the sensor signal
- Amplifier with programmable voltage offset compensation `VPO`.

6.5 ADC

- Single Ended and Fully Differential mode

Table 8: Parameter output amplifier

Parameter	Min.	Nom.	Max.	Unit
Resolution		14		Bit
INL		TBD		LSB
Positive reference voltage (VREFP)		1.8		V
Negative reference voltage (VREFN)		0.6		V
Input voltage single Ended	0		2.4	V
Input voltage differential		±(VREFP-VREFN)		V
Sample rate			1500	KSPS

6.6 Temperature sensor (VTEMP) with ADC

- Providing an output voltage, with lineal temperature dependency.
- The ADC temperature can be read as the temperature reading at `ADCTEMP` register address 34 or as the voltage reading register 41.

Table 9: Temperature sensor parameters

Parameters	Min.	Nom.	Max.	Unit
Operation point: -50°C +25°C +100°C		 310 630 950		 V V V
Rising rate		4.3		mV/K

6.7 Clock generator (CLOCK)

- Generation of the internal clock pulse
- Generation of the basic clock pulse and of the control signals for the sensor

Table 10: Clock generator parameters

Parameter	Min.	Nom.	Max.	Unit
Internal clock frequency CLKINT*		40		MHz
Internal clock temperature stability CLKINT (-40...+105°C)		1700		ppm·K^{-1}
ADC triggering clock	1 / 8192		1/2	CLKINT
Sensor clock (depends of sampling mode)	1 / 96		1 / 24	CLOCK

* Adjustment is performed by the manufacturer

6.8 Sensor control

The setting for the sensor clock is done via the clock divider register at configuration/operation mode register `STPCLKVAL` and can be calculated from:

$$SENSOR\,CLOCK = \frac{CLKINT}{(STPCLKVAL + 1) * 2 * \mathrm{DIV}} \quad [2]$$

The resulting sensor clock is then again dependent on the selected sampling mode `OPM1`, set also at configuration/operation mode register and on the number of working channels. See table 11.

Table 11: Sensor clock division per sampling mode

Sampling mode	One Channel	Two Channel
Single-ended sampling (OPM1 = '0')	DIV = 24	DIV = 48
Dual single-ended sampling (OPM1 = '1')	DIV = 48	DIV = 96

The settings for `STPCLKVAL` and `OPM1` should be selected so that the maximum sensor frequency of 500 KHz is not exceeded.

Table 12: Maximum adjustable sensor frequency as per mode

	Resulting Sensor clock[1]		
STPCLKVAL (Decimal)	Single-ended sampling (OPM1 = '0'), one channel	Dual single-ended sampling (OPM1 = '1'), one channel Single-ended sampling (OPM1 = '0'), two channel	Dual single-ended Sampling (OPM1 = '1'), two channel
0	**833 kHz, NOT VALID**	416 KHz	208 KHz
1	416 KHz	208 KHz	104 KHz
2	277 KHz	138 KHz	69 KHz
...	...	...	...
4095	203 Hz	101 Hz	50 Hz

[1] CLKINT = 40 MHz

Furthermore the piezo mode can be enabled via the sensor control register `PIEZOX` and `PIEZOY`. In piezo mode DISCHARGE will be permanently held at low level.

Hint: *Single-ended sampling: Simple digital conversion of the resulting sensor charge on a single switching edge of the excitation*

Dual single-ended sampling: digital conversion from both *charges generated by the sensors to* both *switching edges of the excitation and the sum of the values*

6.8.1 Timing sensor excitation / normal mode

1-channel, single-ended sampling (OPM1 = '0')

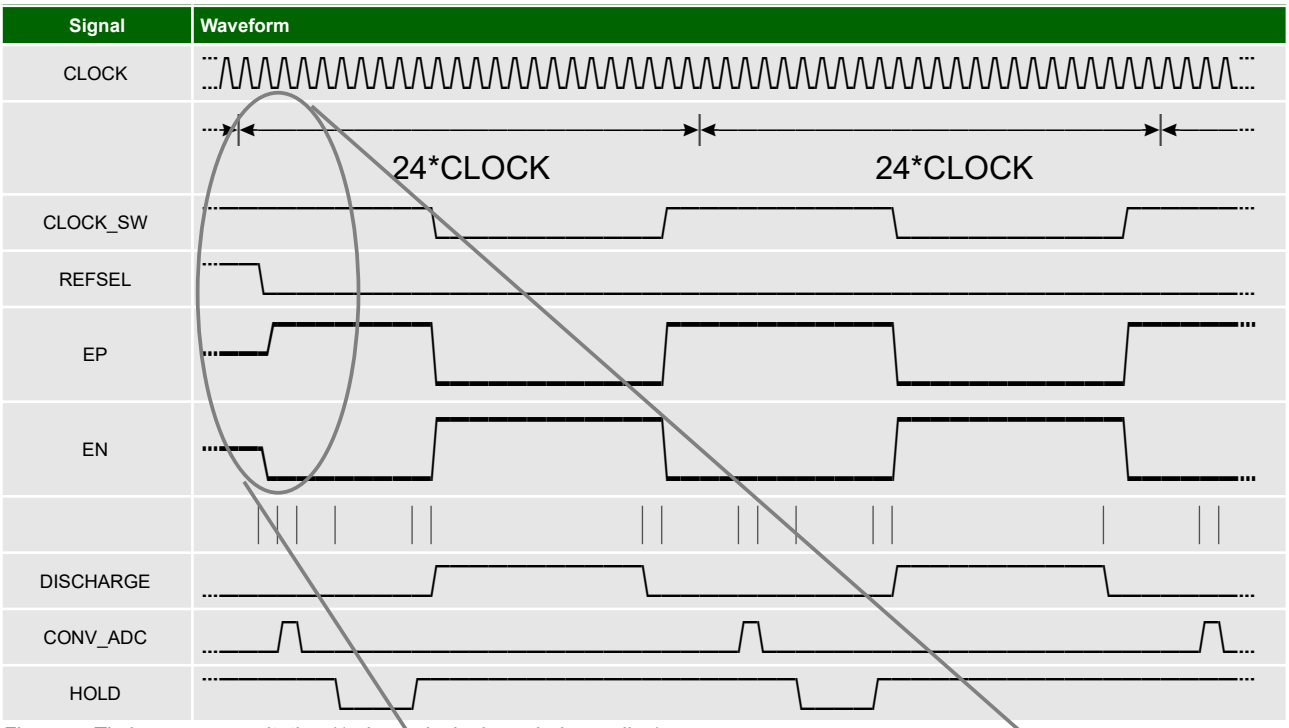


Figure 4: Timing sensor excitation (1-channel, single-ended sampling)

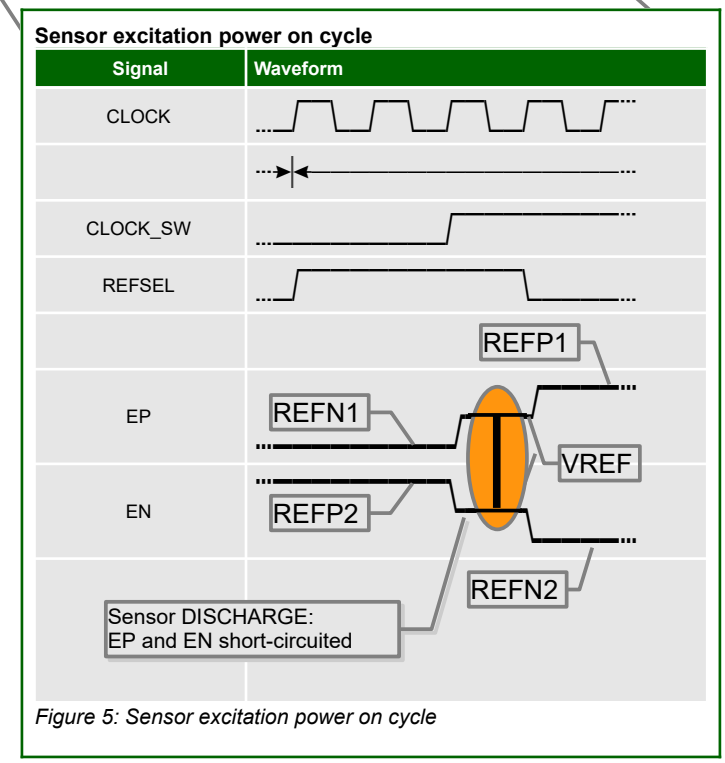


Figure 5: Sensor excitation power on cycle

1-channel, dual single-ended sampling (OPM1 = '1')

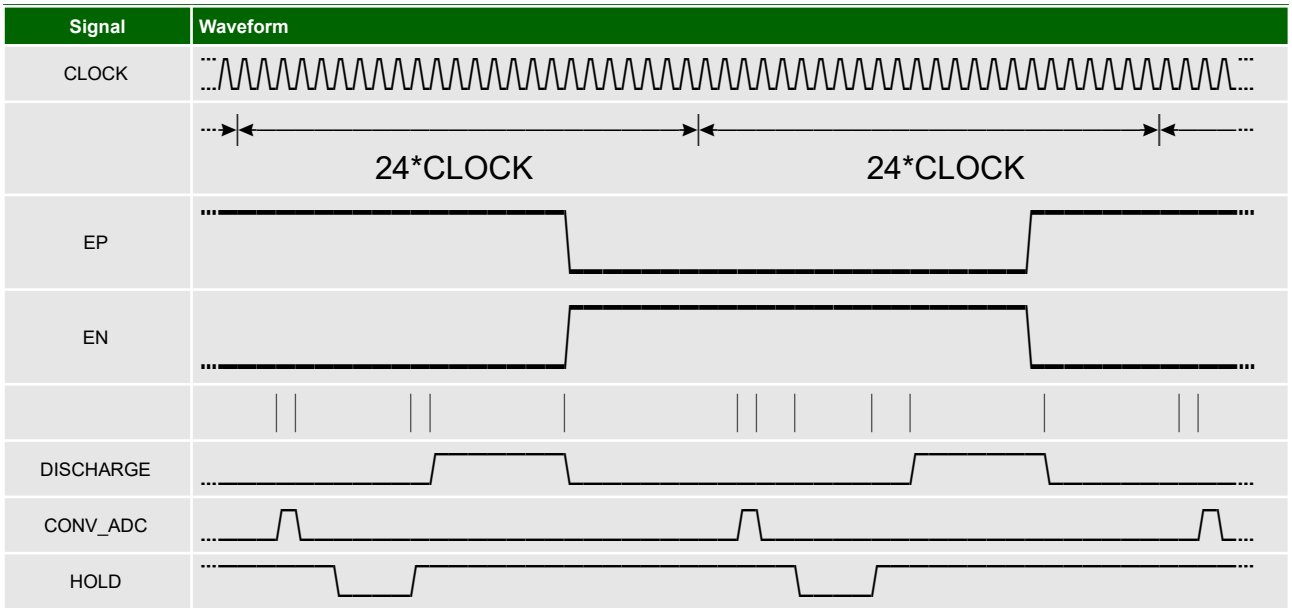


Figure 6: Timing sensor excitation (1-channel, dual single-ended sampling)

2-channel, single-ended sampling (OPM1 = '0')

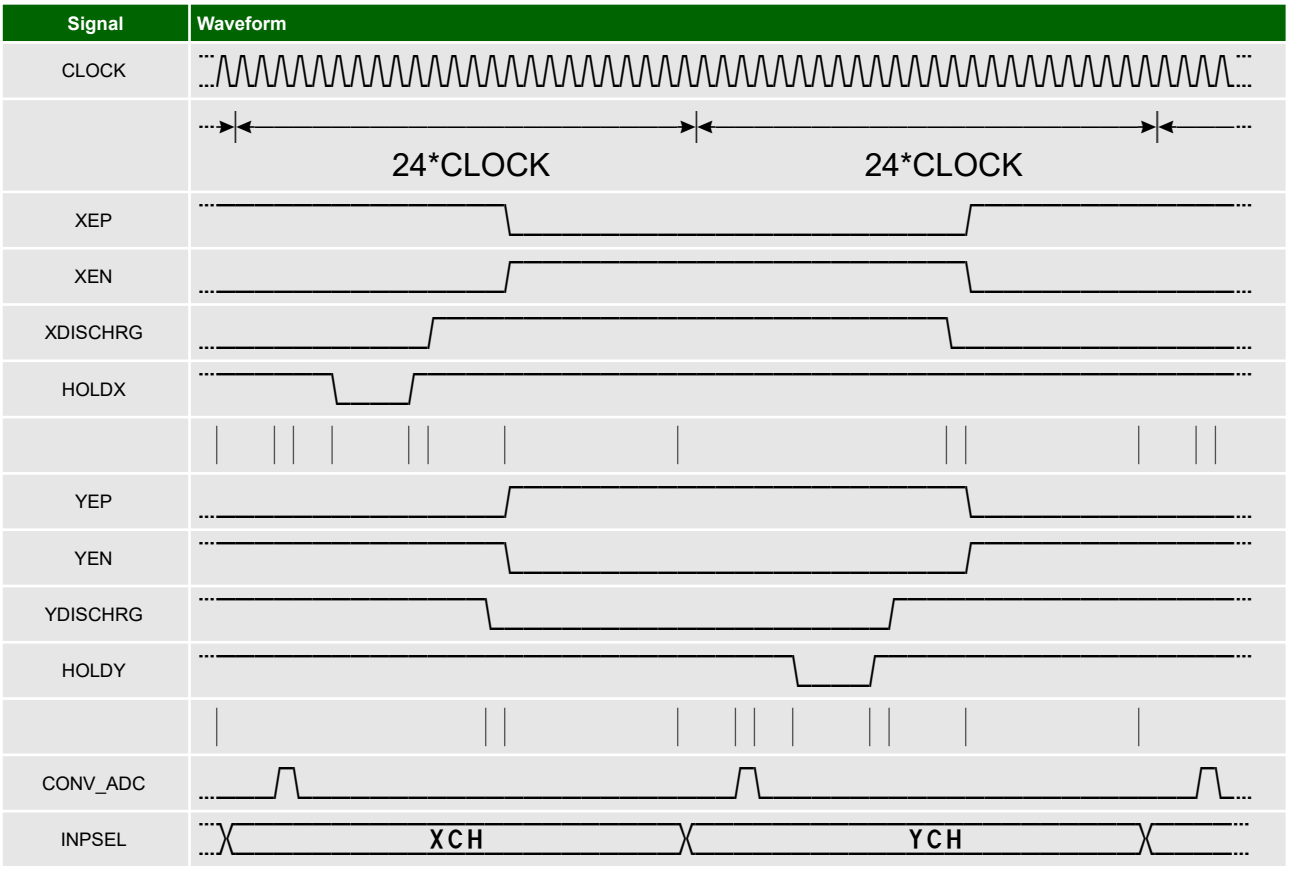


Figure 7: Timing sensor excitation (2-channel, single-ended sampling)

2-channel, dual single-ended sampling (OPM1 = '1')

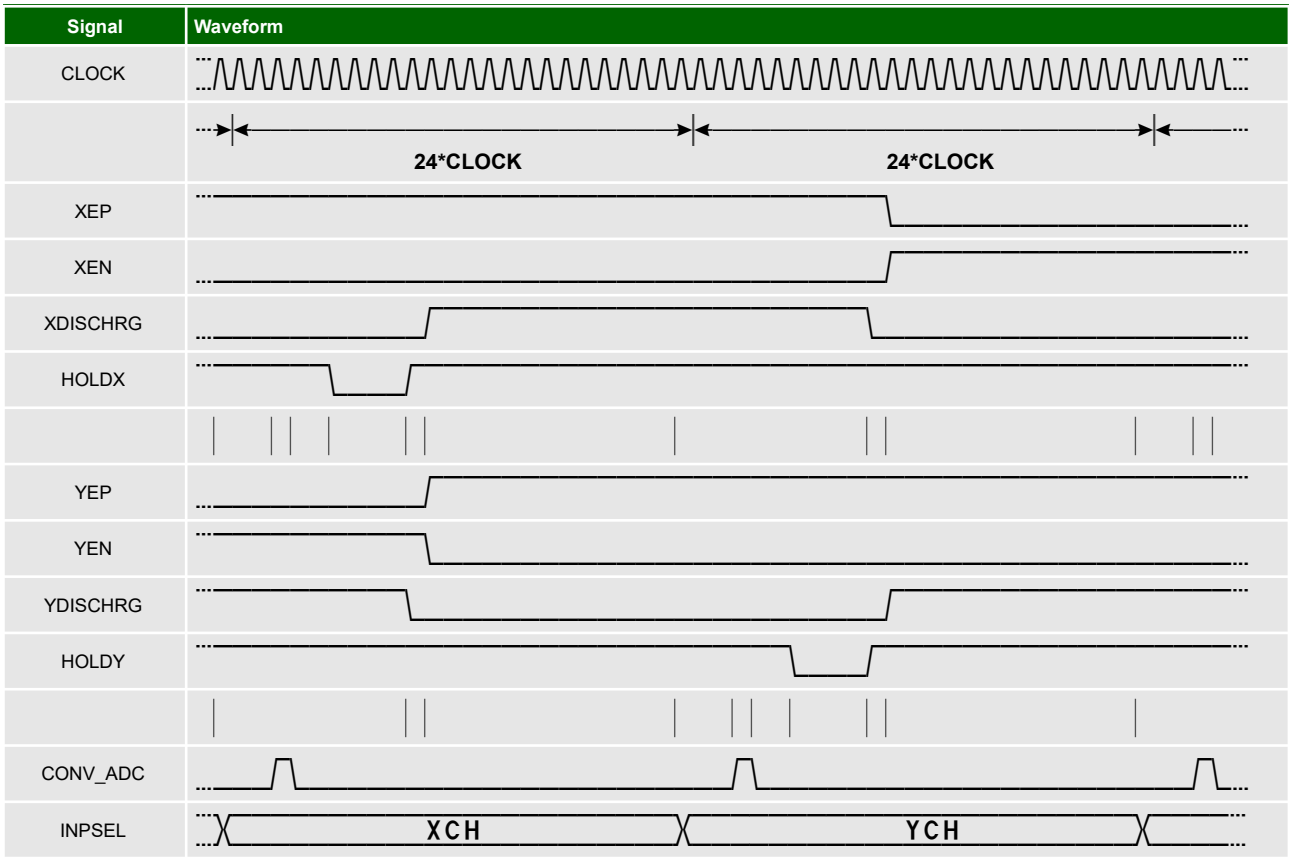


Figure 8: Timing sensor excitation (2-channels, dual single-ended sampling), part 1

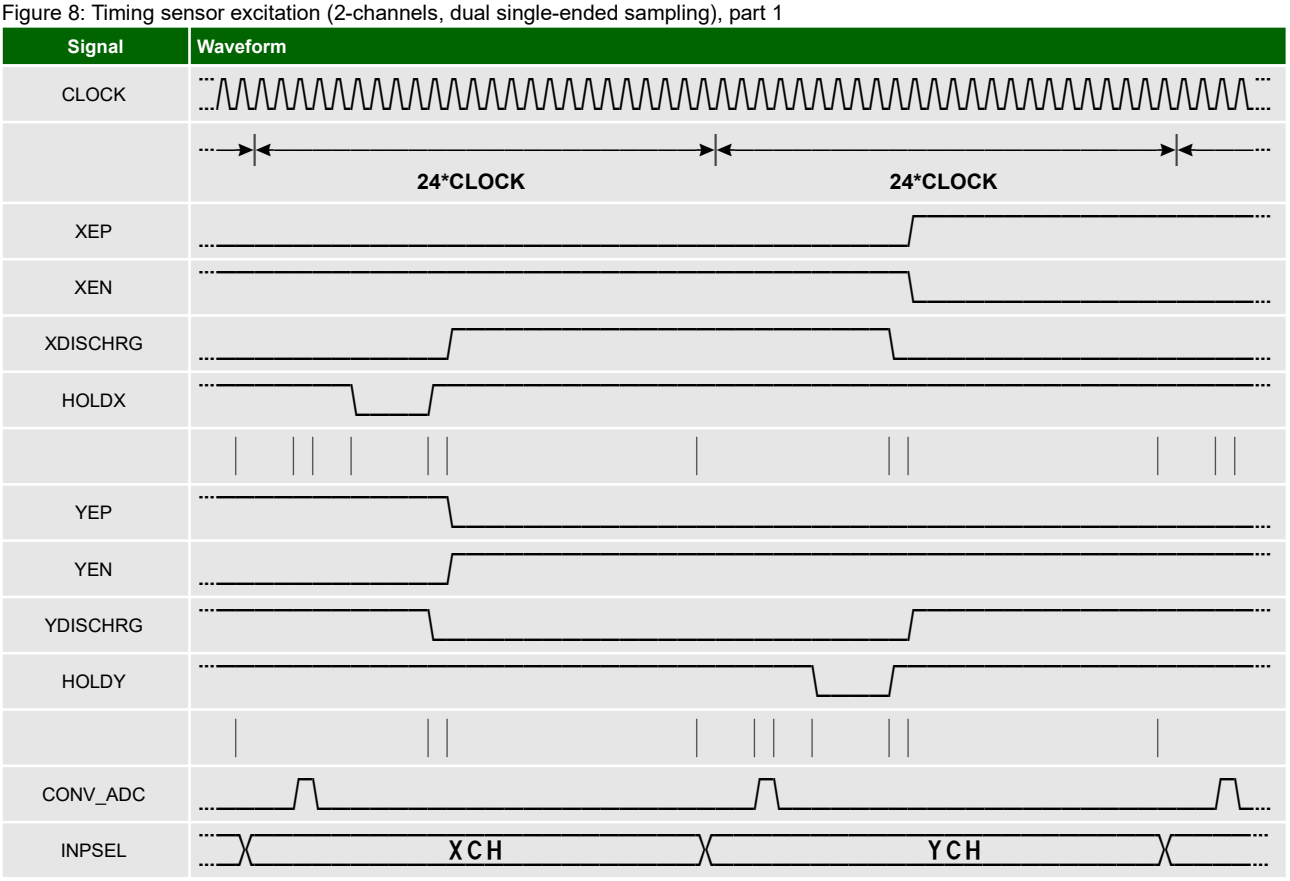


Figure 9: Timing sensor excitation (2-channel, dual single-ended sampling), part 2

6.9 Digital signal processing

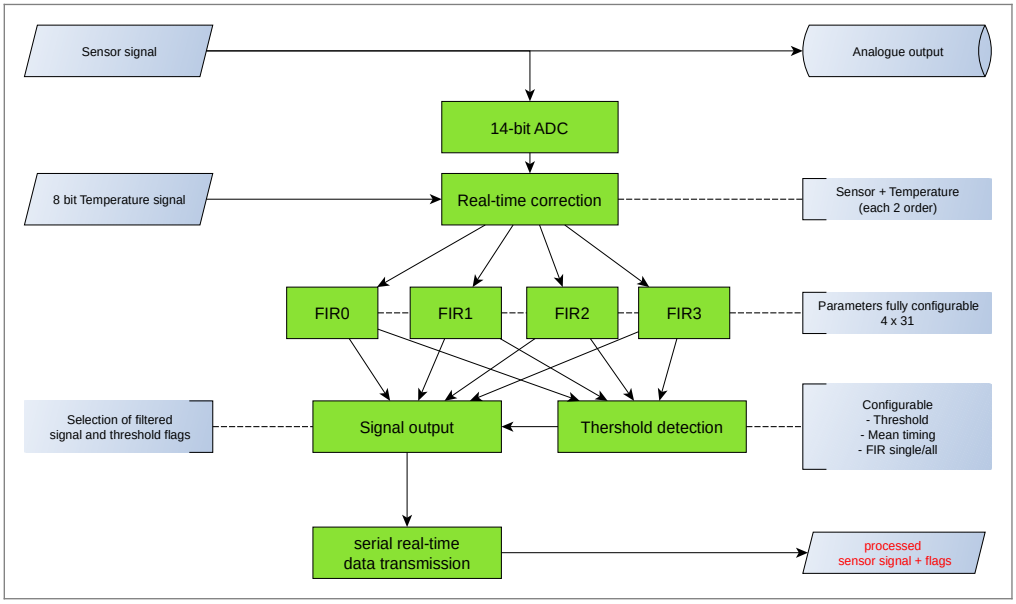


Figure 10: Block diagram digital signal processing

6.9.1 Sensor signal correction

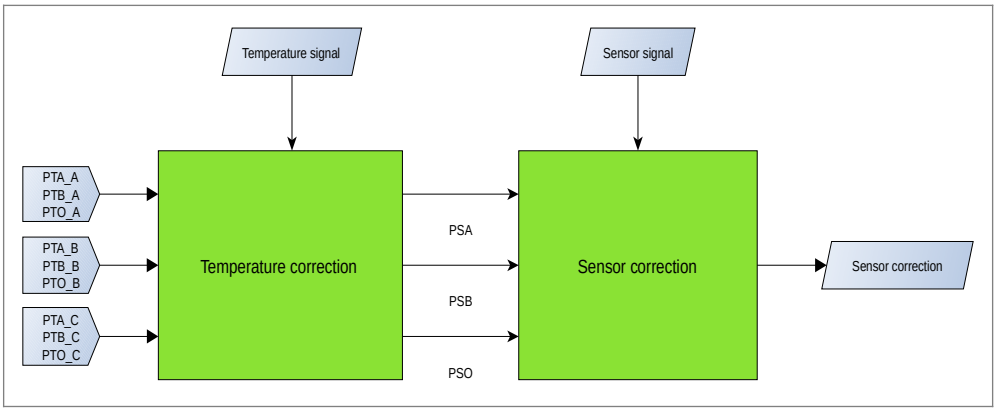


Figure 11: Block diagram sensor signal correction

Both temperature correction and sensor correction are activated via the register `TC_ENA`. At formula [2] from PTA, PTBA, and PTO as well as from the temperature signal the correction parameters PSA, PSB, and PSO are calculated,

$$PS_{A/B/O} = (\mathrm{PTA\_}_{A/B/C}) * temp^2 + (\mathrm{PTB\_}_{A/B/C}) * temp + \mathrm{PTO\_}_{A/B/C} \quad [2]$$

The input parameters PTA, PTB, and PTO are set from its corresponding registers, each 10 bit long. There is also a setting for the scaling factor, `PTSCALE`.

With the resulting values is the sensor signal then corrected by applying the following formula:

$$\mathrm{ADC\_COR} = PSA * |ADC + PSO| * (ADC + PSO) + PSB * (ADC + PSO) \quad [3]$$

6.9.2 FIR-Filter

The integrated signal filtering function consists of four FIR-Filters which are fully configurable, 31 parameters per filter. The filter parameters can be defined using the MATLAB *function firpm ()*

The number of filters for each channel can be selected via the configuration register at XENA_FIR and YENA_FIR. The notation for the filters is FIR0, FIR1, FIR2, and FIR3. For the X-channel will start from FIR0 and then increment. For the Y-channel it will start with the FIR3 and then decrement, see table 13. A FIR-Filter can only be activated for one channel at a time. This means that if any FIR-Filter is assigned to both channels, the values at XENA_FIR and YENA_FIR are disregarded. And the FIR-Filters will be assigned as in the 010 value, FIR0 and FIR1 for the X-channel as well as FIR2 and FIR3 for the Y-channel.

Table 13 FIR-Filter configuration at XENA_FIR and YENA_FIR

Configuration register parameter	Value	Filter			
		FIR0	FIR1	FIR2	FIR3
XENA_FIR (3 bits)	000	OFF	OFF	OFF	OFF
	001	ON	OFF	OFF	OFF
	010	**ON**	**ON**	**OFF**	**OFF**
	011	ON	ON	ON	OFF
	100	ON	ON	ON	ON
YENA_FIR (3 bits)	000	OFF	OFF	OFF	OFF
	001	OFF	OFF	OFF	ON
	010	**OFF**	**OFF**	**ON**	**ON**
	011	OFF	ON	ON	ON
	100	ON	ON	ON	ON

The number of filter parameters (filter order) is set via the corresponding FIR_LEN0/_-LEN3 register at signal correction. A value of 0 will bypass the signal processing of the related FIR-Filter.

The parameters (filter coefficients) are saved in the SRAM. At start up the filter coefficients are transferred from EEPROM to the SRAM.

6.9.3 Threshold detection

If the THRES_EN is activated, the sensor data is then with a threshold reference value compared. This threshold reference value is defined according to the select (ST_MODE/THRESSEL), see 14. Threshold reference values are also programmable. THRESH0 and THRESH1 are 14 bit long and VXPETH and VYPETH 8 bit long. The last two apply only for the self test mode.

The threshold flags will remain high until the number of cycles set at THRES_MAX is reached. Once the cycles are completed, the threshold flags will be activated. Then the THRESHOLD FLAGS will indicate with 1, whether any sensor data is under the threshold reference value. And glitches will be suppressed depending on the THRES_RES_MAX, which designates the number of measurement values cycles to be rejected once the threshold flags are active.

Table 14 Threshold detection flags and reference values

Signal	Address flag	Select	Threshold reference value
ADCX	THRES(0)	ST_MODE=0	THRESH0
		ST_MODE=1	VXPETH
ADCX_COR	THRES(1)	ST_MODE=0	THRESH0
		ST_MODE=1	VXPETH
ADCY	THRES(2)	ST_MODE=0	THRESH1
		ST_MODE=1	VYPETH
ADCY_COR	THRES(3)	ST_MODE=0	THRESH1
		ST_MODE=1	VYPETH

Signal	Address flag	Select	Threshold reference value
FIR_OUT0	THRES(4)	THRESSEL(0)=0	THRESH0
		THRESSEL(0)=1	THRESH1
FIR_OUT1	THRES(5)	THRESSEL(1)=0	THRESH0
		THRESSEL(1)=1	THRESH1
FIR_OUT2	THRES(6)	THRESSEL(2)=0	THRESH0
		THRESSEL(2)=1	THRESH1
FIR_OUT3	THRES(7)	THRESSEL(3)=0	THRESH0
		THRESSEL(3)=1	THRESH1

6.9.4 Real-time data transmission

The real-time data transmission is activated via the OPM2. As a result the AM-CVC2D functions as SPI master, as long as no data transmission is requested from the master at SEN. When a data request is generated from the master while a data transmission is being executed, the current data transmission is immediately stopped and all values that were loaded at the buffer are discarded.

SPI master

The output nCS_MA works as the chip select. The clock is active at the ouput SCK_MA, and the data is send as usual via the MOSI now operating as output and also at MISO, see 22. The clock rate from the transmission is set at the SPIMACLK. It has a range of 40 MHz to 156 KHz, for the values 1 to 255 at register. In order to reduce the data rate the parameter DMA_DIV will determine to transmit every n-value. From every 2nd value to every 15th value possible.

At this interface the ADC values, the corrected ADC values, and FIR values can be sent. New data values do not have to be polled. Via the register SENDREG is selected which values should be send. See table 15.

Table 15*: Data select SENDREG*

SENDREG (7:0)	Data select at SPI real-time data transmission	
Bit 0 = 1	ADCX	ADC value X-channel
Bit 1 = 1	ADCX_COR	ADC corrected value X-channel
Bit 2 = 1	ADCY	ADC value Y-channel
Bit 3 = 1	ADCY_COR	ADC corrected value Y-channel
Bit 4 = 1	FIR_OUT0	Output value FIR0
Bit 5 = 1	FIR_OUT1	Output value FIR1
Bit 6 = 1	FIR_OUT2	Output value FIR2
Bit 7 = 1	FIR_OUT3	Output value FIR3

Each data transmission is made up of 24 bit data: an operation code (OP-code), threshold flag from value, and the data value itself. See table 16. The parameter at ADTX defines whether the data is send as a single 24 bit long transmission (ADTX = 1) or as three 8 bit long transmissions (ADTX = 0). The data is buffered until new data of the same type comes.

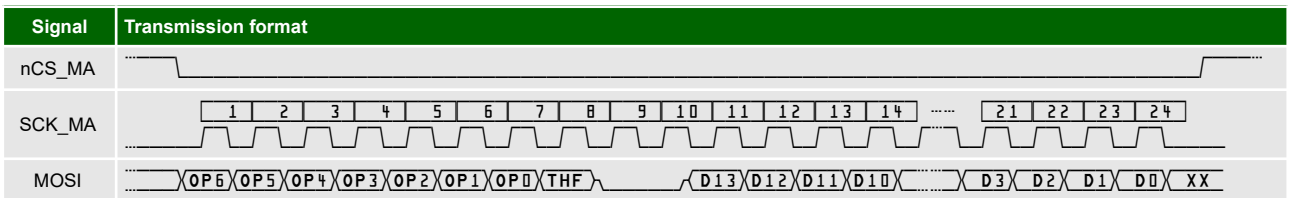


Figure 12: SPI master 24 bit transmission

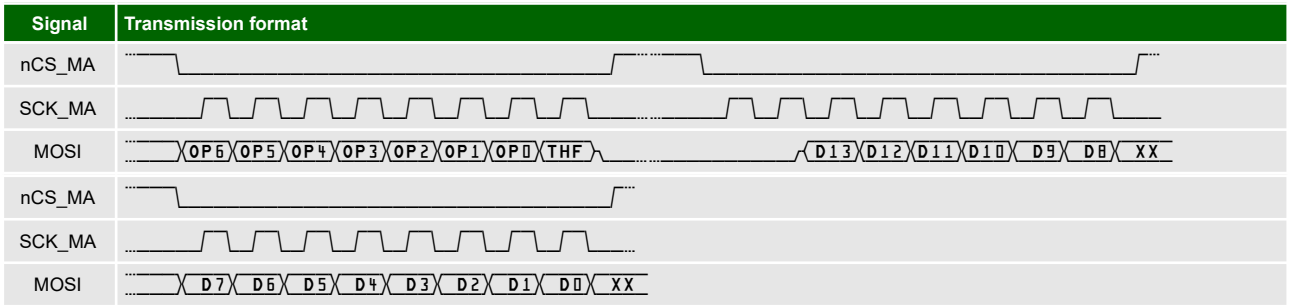


Figure 13: SPI master 3 x 8 bit transmission

The transmission is MSB bit first. The OP code is 7 bits long and works as an identifier for each data that is being sent. For the three 8 bit transmissions, the first byte to be sent is the data 3, following data 2, and the last byte is data 1.

Table 16: Real-time data transmission, data at MOSI/MISO

OP code (Bit 23:20)	OP code (Bit 19:17)	THF (Bit 16)	Data (Bit 15:14)	Data (Bit 13:0)
DATA3 (23:16)			DATA2(15:8), DATA1(7:0)	
0000	000	THRES(0)	00	ADCX
0010	000	THRES(1)	00	ADCX_COR
0100	000	THRES(2)	00	ADCY
0110	000	THRES(3)	00	ADCY_COR
1000	000	THRES(4)	00	FIR_OUT0
1010	000	THRES(5)	00	FIR_OUT1
1100	000	THRES(6)	00	FIR_OUT2
1110	000	THRES(7)	00	FIR_OUT3

I²C real time data transmission

The I²C interface can also send the data at real time. First the `OPM2`, `DMA_DIV`, and `SENDREG` bits (7:0) have to be configured.

The real time data can be read by setting the read register address for the DMA with the proper operation code of the I²C, section 7.2. Then three bytes will be read out, data bytes have the same designation as in the SPI transmission. See table 16.

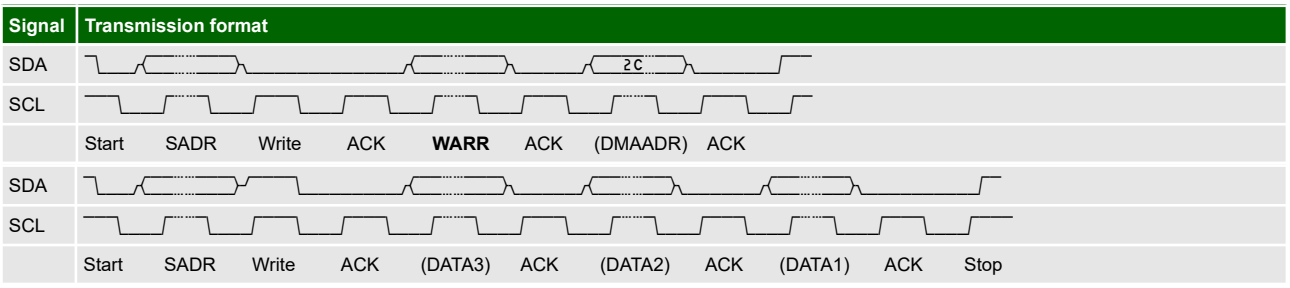


Figure 14: I²C real time data read 3 x 8 bit transmission

6.10 SIL block

The status SIL register monitors the X/Y-channels, temperature, and voltage. The channel monitoring compares the difference *ADCX - ADCY* with the set threshold at `FAILTH` when `SIL_ENA` and `CHN_ENA` are activated. Resulting error is reported at CHNFAIL bit.

At the temperature monitoring, the ADC temperature value is compared with the value at `SIL_TMP`. If the maximal value is exceeded then the error is shown at bit TMP_FAIL.

Same for the voltage monitoring, the VDDFAIL bit indicates when the voltage is out of the tolerated values. (V_{DD} > +10%, V_{DD} < -10%).

For the self test mode, `ST_MODE` = 1. The number of test cycles is taken from the register `STCYC`. The threshold values are then set with `VXPETH` and `VYPETH`.

The SIL register also includes the threshold flags. See SIL STATUS.

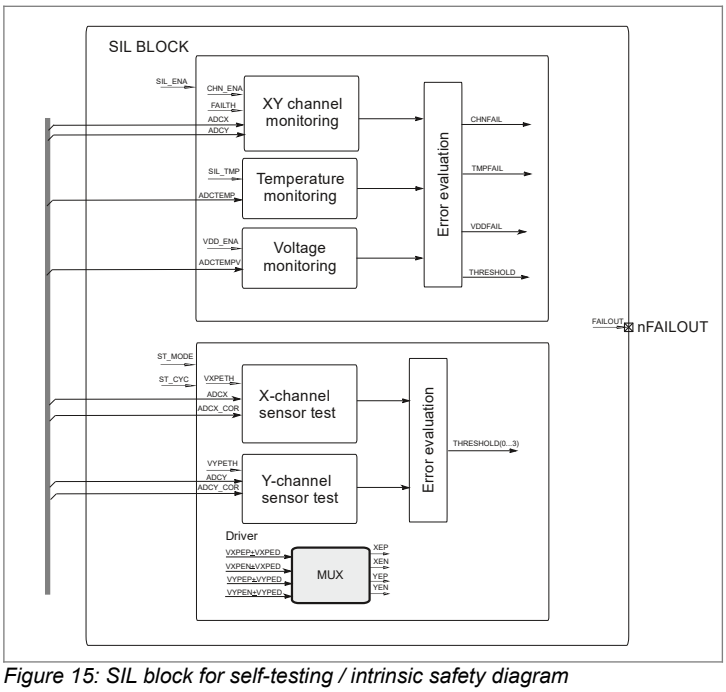


Figure 15: SIL block for self-testing / intrinsic safety diagram

7 Interfaces

The MSSC can be operated through two interfaces, via SPI or I²C interface. The different modes can be deployed via pin IFC_SEL. A high level will activate the SPI interface hence a low level the I²C interface.

7.1 SPI-Interface

The AM-CVC2D operates in normal mode as a SPI slave. Every access via the SPI interface is 16 bit long with MSB first, and will begin when the SEN signal falls to a low level. The IC sends data via the MISO signal and receives data via the MOSI signal. Furthermore data will be read with the rising edge of SCK_MA (shift in) and send with the SCK_MA falling edge.

7.1.1 SPI signals

Table 17: SPI signals

Signal	Meaning	Direction	
		Master mode	Slave mode
SCK_MA	Clock signal with rising edge the data at MOSI is sampled with falling edge the data at MISO is modified	OUT	IN
SEN	Enable Low: interface is enabled High: interface is disabled	-	IN
nCS_MA	Chip select master mode, low active	OUT	-
MOSI	Master out slave in Data input / Data output	OUT	IN
MISO	Master in slave out Data output and status signal	OUT	OUT

The end of the transmission is indicated when the SEN signal goes back to a high level. The AM-CVC2D acknowledges this action with low level at MISO (busy-status) as long as the transmission is being executed. The completion of the transmission is acknowledged with a high level at MISO (ready-status). Then can the next transmission begin. The SPI interface works asynchronously to the internal clock.

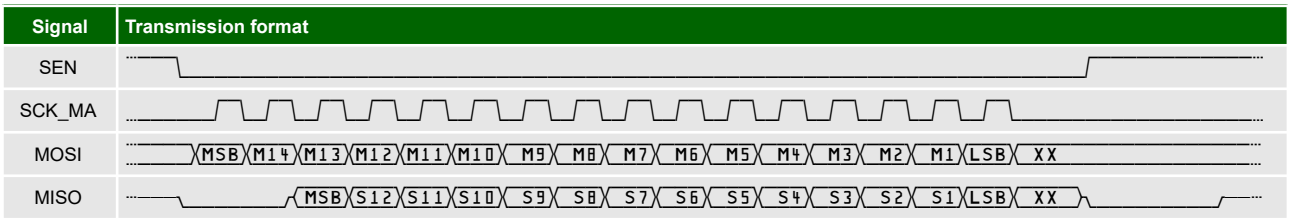


Figure 16: SPI transmission format

The SPI interface performs the write/read accesses of registers or EEPROM/SRAM via EEPDATA register by executing a sequence of different OP-codes.

7.1.2 SPI protocol

Table 18: SPI protocol, MOSI data

OP-Code at MOSI	Description	Signal MOSI bits															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		OP-Code				ADDRESS/DATA											
NOP	Read data (14Bit)	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X
WD	Write data	0	1	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WAR	Write RD/WR Address to Register	1	0	X	X	X	X	X	X	X	X	A5	A4	A3	A2	A1	A0
WAER	Write Addr. A [7:0] EEPROM/SRAM read	1	1	0	X	X	X	X	X	A7	A6	A5	A4	A3	A2	A1	A0
WAEW	Write Addr. A[7:0] EEPROM/SRAM write	1	1	1	X	X	X	X	X	A7	A6	A5	A4	A3	A2	A1	A0

Table 19: SPI protocol, MISO data

OP-Code at MISO	Description	Signal MISO bits															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		DATA															
ALL	For each access the MISO sends the actual data from the read register	0	0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 20: SPI protocol, designation

Bits	Designation	Description
A(7:0)	Address	Specifies an address within the ICs content, for the access of the configuration registers, SRAM, or EEPROM. At registers only bits (5:0) are relevant. MSB first
D(13:0)	Data	Read and write data 14 bit, MSB first

Hint: *The high level at MISO occurs right after the edge change of* `SEN` *from low to high. For this reason in order to execute the OP-codes* ***WAEW*** *and* ***WAER*** *should also be taken into account the signal BUSY before any other EEPROM-Operation is realized.*

The state bits EESTBY, STARTUP, EEPBUSY from EEPROM are send when the register 18 is read at bits 13, 12 and 11.

When an access at EEPROM is done, the status bit EESTBY changes after at least 3 clocks of EECLK from the rising edge of `SEN`*.*

7.1.3 Register access

Register write

Table 21: Sequence register write access

SPI OP-Code	Description of the internal process
WAR with Address = register address	The internal address pointer is set with the register address
WD with Data = register data	Data is saved at the previously addressed data register

Register read

Table 22: Sequence register read access

SPI OP-Code	Description of the internal process
WAR with Address = register address	The internal address pointer is set with the register address
NOP	Data from previously addressed register is sent at MISO

7.1.4 SRAM and EEPROM access

The EEPROM and SRAM can be only accessed indirectly via register access `EEPDATA`. To differentiate between an EEPROM and SRAM access the `RAMRWSPI` should be set.

Table 23: EEPROM/SRAM access select

RAMRWSPI value	Access to:
RAMRWSPI= 0	EEPROM access
RAMRWSPI= 1	SRAM access for filter coefficients

The bit for `RAMRWSPI` should be written by executing the register access without changing the content of the rest bit values. Such sequence is suggested:

Table 24: Sequence: RAMRWSPI

SPI OP-Code	Description of the internal process
WAR with Address = register address RAMRWSPI = 1Dh	The internal address pointer is set with the register address from RAMRWSPI
NOP	Data from 1Dh register is sent at MISO
WD with Data = value to be stored	Bit 13: 1 = SRAM, 0 = EEPROM, the rest from the data previously read from MISO so that other configuration register bits remain the same.

EEPROM/SRAM write

Table 25: Sequence EEPROM/SRAM write access

SPI OP-Code	Description of the internal process
WAR with Address = register address EEPDATA = 06h	The internal address pointer is set with the register address from EEPDATA
WD with Data = value to be stored	Data is stored at the EEPDATA register.
WAEW write Address = EEPROM/SRAM address	Data from EEPDATA register is stored at the EEPROM/SRAM received address.

EEPROM/SRAM read

Table 26: Sequence EEPROM/SRAM read access

SPI OP-Code	Description of the internal process
WAER mit Address = EEPROM/SRAM address	Data is read-out from the EEPROM/SRAM address and the data stored at EEPDATA register stored.
WAR with Address = register address EEPDATA = 06h	The internal address pointer is set with the register address from EEPDATA
NOP	Data from EEPDATA register is sent at MISO

The addressing of the non-volatile storage elements of the EEPROM is structured as the configuration registers. (See Configuration registers)

Hint: *Changes in the EEPROM configuration are effective after a reset, power on.*

For consecutive Read and write of multiple registers or EEPROM content, the accesses can be repeated.

7.1.5 SPI specifications

Table 27: SPI timing and electrical specifications

Parameter	Min.	Nom.	Max.	Unit
Clock SCLK			2	MHz
Duty cycle SCLK	40	50	60	%
VIH (SEN, SCLK, MOSI)	2.1			V
VIL (SEN, SCLK, MOSI)			0.8	V
VOH (MISO_/BUSY) with 4 mA	2.6			V
VOL (MISO_/BUSY) with 4 mA			0.5	V

7.2 I²C-Interface

With a low level at IFC_SEL is the I²C interface activated. A 50 ns spike filter can be via the configuration register I2C_SPIKE enabled. In I²C mode the pin MOSI works as the SDA line and the pin SEN as the SCL I²C clock.

7.2.1 I²C signals

Table 28: I²C signals

Signal	Pin	Meaning	Direction
SDA	MOSI	Data line	IN/OUT
SCL	SEN	Clock line	IN

7.2.2 I2C protocol

The 7 bit slave address for the I²C is selected according to the values at pins ADDR1 and ADDR0. There is a fixed slave address when ADDR1 and ADDR0 have an input value of 11. Additionally the other addresses are defined with the two bits from I2C_SADR_H.

Table 29: I2C slave address configuration

ADDR1	ADDR0	I²C Slave address (7:0)		
		Bits (6:5)	Bits (4:3)	Bits (2:0)
0	0	10	I2C_SADR_H	000
0	Z	10	I2C_SADR_H	001
0	1	10	I2C_SADR_H	110
Z	0	10	I2C_SADR_H	010
Z	Z	10	I2C_SADR_H	011
Z	1	10	I2C_SADR_H	100
1	0	10	I2C_SADR_H	111
1	Z	10	I2C_SADR_H	101
1	1	10	10	000

The I²C interface performs the write/read accesses of registers or EEPROM/SRAM EEPDATA register by executing different OP-codes. All are considered write accesses when the pointer address is written.

Table 30: I2C OP codes

OP-Code	Description	7	6	5	4	3	2	1	0
WD	Write Data in addressed write register	0	1	X	X	X	X	X	X
WARW	Write Address ADR at write Register pointer, Write data at write register	1	0	1	X	X	X	X	X
WARR	Write Address ADR at Read Register pointer	1	0	0	X	X	X	X	X
WAER	Write data from ADR EEPROM/SRAM to EEPDATA	1	1	0	X	X	X	X	X
WAEW	Write register EEPDATA to EEPROM/SRAM at ADR	1	1	1	X	X	X	X	X

A write/read access via the I²C interface is realized following the format:

S/Sr	SADR +W=0	ACK	OPC	ACK	(ADR)	ACK	(DATA)	ACK	(DATA)	ACK	P

I²C format write access

S/Sr	SADR +W=1	ACK	(DATA)	ACK	(DATA)	ACK	P	

I²C format read access

Table 31: Format meaning

	Meaning		Meaning
S/Sr:	Start condition/ re-start condition	OPC	OP-code
SADR	slave address, 7 bit	ADR	Address, depends on access WRADR, RDADR EEPADR[1].
W	write bit, W= 0 write, W= 1 read	DATA	8 bit
ACK	Acknowledge	P	Stop condition

[1] EEPADR applies to EEPROM or SRAM address.

7.2.3 Register access

Register write1:

Signal	Transmission format
SDA	
SCL	
	Start SADR Write ACK **WD** ACK (DATA2) ACK (DATA1) ACK Stop

Figure 17: I²C register write 1

Register write2:

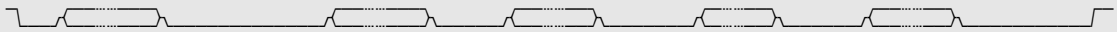
Signal	Transmission format
SDA	
SCL	
	Start SADR Write ACK **WARW** ACK (WRADR) ACK (DATA2) ACK (DATA1) ACK Stop

Figure 18: I²C register write 2

Register read:

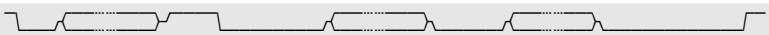
Signal	Transmission format
SDA	
SCL	
	Start SADR Write ACK **WARR** ACK (RDADR) ACK Repeated Start
SDA	
SCL	
	Start SADR Write ACK (DATA2) ACK (DATA1) ACK Stop

Figure 19: I²C register read

7.2.4 EEPROM/SRAM access

An EEPROM/SRAM access is done via the register `EEPDATA`.

EEPROM/SRAM write:

The write access is performed in two steps. The first one is where the data at the `EEPDATA` (register address h06) is written and the second step is where the `EEPDATA` register data is stored at the SRAM/EEPROM addres (EEPADR).

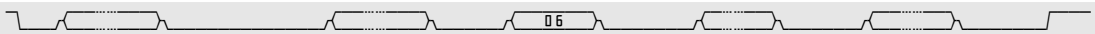
Signal	Transmission format
SDA	
SCL	
	Start SADR Write ACK **WARW** ACK (EEPDATA_ADR) ACK (DATA2) ACK (DATA1) ACK Repeated Start
SDA	
SCL	
	Start SADR Write ACK **WAEW** ACK (EEPADR) ACK Stop

Figure 20: I²C EEPROM/SRAM write

EEPROM/SRAM read:

The read access is also performed in different steps. First one is to write at `EEPDATA` register the data from the address from EEPROM/SRAM (EEPADR). Then carry out a normal read register access from the `EEPDATA` register.

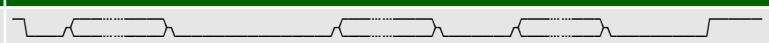
Signal	Transmission format
SDA	
SCL	
	Start SADR Write ACK **WAER** ACK (EEPADR) ACK Repeated Start
SDA	
SCL	
	SADR Write ACK **WARR** ACK (EEPDATA_ADR) ACK Repeated Start
SDA	
SCL	
	Start SADR Write ACK (DATA2) ACK (DATA1) ACK Stop

Figure 21: I²C EEPROM/SRAM read

The SDA line data has designation according to the actual operation code. For address data, an 8 bit transmission is enough. While for the data transmission the bits are assigned as in table for the two transmissions:

Table 32: I²C SDA data

OP-Code	DATA/ADDRESS	SDA: DATA bits															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		DATA2								DATA1							
-	Data 14 bits	X	X	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
WARW WARR	Address: register pointer									X	X	A5	A4	A3	A2	A1	A0
WAEW	Address EEPADR									A7	A6	A5	A4	A3	A2	A1	A0

For the **WAEW** and **WAER** *should also be taken into account the signal BUSY before any other EEPROM-Operation is realized.*

8 Register and internal memory

8.1 Configuration registers

Table 33: Configuration registers assignment

Register address		Std. Value	Bit													
			13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	00h	0000 h	VTSELX									VXP				
1	01h	0000 h		OCNCX		XPHASE						VXN				
2	02h	0000 h	XCINT										VXPED			
3	03h	0080 h	AVGX		CHENA_X	PIEZOX		PDX		XCOFF_SW			XCOFF			
4	04h	0000 h	VTSELY									VYP				
5	05h	0000 h		OCNCY		YPHASE						VYN				
6	06h	0000 h	EEPDATA													
7	07h	0000 h	YCINT										VYPED			
8	08h	0000 h	AVGY		CHENA_Y	PIEZOY		PDY		YCOFF_SW			YCOFF			
9	09h	0000 h		PDREF	ADCPD	SH_ENA						VPO				
10	0Ah	0000 h		OPM1						STPCLKVAL						
11	0Bh	0000 h						ST_MODE				VXPETH				
12	0Ch		STCYC									VYPETH				
13	0Dh		SIL_TMP			VDD_ENA	CHN_ENA	SIL_ENA				FAILTH				
14	0Eh				THRES_EN	THRES_RES_MAX						THRES_MAX				
15	0Fh		THRESH0													
16	10h		THRESH1													
17	11h		THRESEL									PTA_A				
18	12h		EESTBY	STARTUP	EEPBUSY	TC_ENA						PTA_B				
19	13h											PTA_C				
20	14h											PTB_A				
21	15h											PTB_B				
22	16h											PTB_C				
23	17h											PTO_A				
24	18h		PTSCALE									PTO_B				
25	19h		TST									PTO_C				
26	1Ah			XENA_FIR					FIR_LEN0				FIR_LEN1			
27	1Bh			YENA_FIR					FIR_LEN2				FIR_LEN3			
28	1Ch				I2C_SPIKE	ADTX		I2C_SADR_H				SPIMACLK				
29	1Dh		RAMRWSPI	OPM2		DMA_DIV						SENDREG				
30	1Eh		EECLKADJ						CLKADJ				VREF			

READ & WRITE | READ ONLY | RESERVED | MANUFACTURER SETTING

The content of the configuration registers is stored at the EEPROM with the same address.

8.2 Data registers

Table 34: Data registers assignment

Register address		Bit													
		13	12	11	10	9	8	7	6	5	4	3	2	1	0
32	20h	ADCX													
33	21h	ADCY													
34	22h	ADCTEMP (temperature)													
35	23h	ADCX_COR													
36	24h	ADCY_COR													
37	25h	FIR_OUT0													
38	26h	FIR_OUT1													
39	27h	FIR_OUT2													
40	28h	FIR_OUT3													
41	29h	ADCTEMP (voltage)													
42	2Ah						SIL STATUS								
							CHNFAIL	TMPFAIL	VDDFAIL	THR(7)	THR(6)	THR(5)	THR(4)	THR(3)	THR(1)
43	2Bh							THRESHOLD FLAGS							

READ ONLY | RESERVED | STATUS & FLAGS

8.3 SRAM – Buffer for FIR filter coefficients

Table 35: SRAM: FIR coefficients buffer

Memory address	Content	Description
0x00 .. 0x1E	h0(0) .. h0(30)	Filter FIR0 coefficients (max. 31 coefficients)
0x1F	-	RESERVED
0x20 .. 0x3E	h1(0) .. h1(30)	Filter FIR1 coefficients (max. 31 coefficients)
0x3F	-	RESERVED
0x40 .. 0x5E	h2(0) .. h2(30)	Filter FIR2 coefficients (max. 31 coefficients)
0x5F	-	RESERVED
0x60 .. 0x7E	h3(0) .. h3(30)	Filter FIR3 coefficients (max. 31 coefficients)
0x7F - 0xFF	-	RESERVED

8.4 EEPROM content

Table 36: EEPROM: configuration registers and SRAM

Memory address	Content	Description
0x00 .. 0x1E	REG0 .. REG30	Configuration registers
0x1F .. 0x80	-	RESERVED
0x81 .. 0x9F	h3(30) .. h3(0)	Filter FIR3 coefficients (max. 31 coefficients)
0xA0	-	RESERVED
0xA1 .. 0xBF	h2(30) .. h2(0)	Filter FIR2 coefficients (max. 31 coefficients)
0xC0	-	RESERVED
0xC1 .. 0xDF	h1(30) .. h1(0)	Filter FIR1 coefficients (max. 31 coefficients)
0xE0	-	RESERVED
0xE1 .. 0xFF	h0(30) .. h0(0)	Filter FIR0 coefficients (max. 31 coefficients)

8.5 Configuration registers description

8.5.1 Clock configuration / Operating modes registers

Table 37: Clock configuration and operating modes registers

Register address	Parameter name	Number of bits	Bit position	Format	Value	Description
28	SPIMACLK	8	7:0	decimal	1 .. 255	Clock divider for SCLK for real-time data transmission Range: 1...255 40 MHz … 156 kHz
10	STPCLKVAL	12	11:0	decimal	0 … 4095	Clock adjustment sensor excitation, see table 12
29	SENDREG	8	7:0	bit	Bit 0 = 1 Bit 1 = 1 Bit 2 = 1 Bit 3 = 1 Bit 4 = 1 Bit 5 = 1 Bit 6 = 1 Bit 7 = 1	Data select at SPI/I²C real-time data transmission ADCX ADCX_COR ADCY ADCY_COR FIR_OUT0 FIR_OUT1 FIR_OUT2 FIR_OUT3
28	ADTX	1	10	bit	0 1	Format SPI real-time data transmission 24-bit frames 8-bit frames
10	OPM1	1	12	bit	0 1	Internal operation mode single-ended conversion dual single-ended conversion
29	OPM2	1	12	bit	0 1	SPI/I²C real time data transmission disabled enabled
3	CHENA_X	1	11	bit	0 1	Sensor X-channel enable X-channel deactivated X-channel activated
8	CHENA_Y	1	11	bit	0 1	Sensor Y-channel enable Y-channel deactivated Y-channel activated
29	DMA_DIV	4	11:8	binary	0010 0011 … 1111	Data rate reduction factor at SPI/I²C real-time data transmission 2nd value 3rd value …. 15th value
28	I2C_SPIKE	1	11	bit	0 1	I2C 50ns spike filter spike filter deactivated spike filter activated
28	I2C_SADR_H	2	9:8	-	-	I2C Slave address bits (4:3), see Table 29

8.5.2 Sensor control registers

Table 38: Sensor control registers

Register address	Parameter name	Number of bits	Bit position	Format	Value	Description
0 1	VXP VXN	10	9:0	decimal	0 1 ... 1023	Amplitude sensor excitation X-channel range: (2*VREF .. 0), step size: 0.001955 2*VREF 1.99*VREF ... 0
4 5	VYP VYN	10	9:0	decimal	0 1 ... 1023	Amplitude sensor excitation Y-channel range: (2*VREF .. 0), step size: 0.001955 2*VREF 1.99*VREF ... 0
2 7	VXPED VYPED	7	6:0	-	Bit (6) = 1 Bit (6) = 0 Bit (5:0)= 000000 000001 … 111111	Detuning of the sensor excitation's amplitude for self test X/Y-channel Detuning positive Detuning negative Detuning bits range: see table 6 for examples. 0 8 … 504
2 7	XCINT YCINT	7	13:7	decimal	0 1 127	Adjustment of the integration capacitance channel X/Y charge amplifier, step size: 0.1pF 0... pF 0.1 pF ... 12.7 pF
3 8	XCOFF YCOFF	7	6:0	decimal	0 1 ... 127	Adjustment of the offset capacitance channel X/Y charge amplifier, Step size: 0.025 pF 0 pF 0.025 pF ... 3.175 pF
1 5	XPHASE YPHASE	1	10	bit	0 1	Phase adjustment of the sensor excitation Phase normal Phase rotated
3 8	XCOFF_SW YCOFF_SW	1	7	bit	0 1	Switch for the offset capacitance reference X-channel XEP, Y-channel YEP X-channel XEN, Y-channel YEN
3 8	PDX PDY	2	9:8	bit	Bit 0 = 1 Bit 1 = 1	Select for analogue power down X/Y-channel Sensor excitation power down Charge amplifier power down
1 5	OCNCX OCNCY	2	12:11	binary	00 01 10 11	Switch between internal and external offset cancelling. No offset cancelling Internal offset activated External offset activated Not possible to activate both
3 8	PIEZOX PIEZOY	1	10	bit	0 1	Piezo mode disabled, DISCHARGE 1 Piezo mode enabled, DISCHARGE 0

8.5.3 Sensor monitoring / SIL registers

Table 39: Sensor monitoring / SIL registers

Register address	Parameter name	Number of bits	Bit position	Format	Value	Description
13	SIL_ENA	1	8	bit	0 1	SIL Disabled Enabled
13	CHN_ENA[1]	1	9	bit	0 1	Channel monitoring SIL 0 = Disabled 1 = Enabled
13	SIL_TMP	3	13:11	binary	000 001 010 011 100 101 110 111	Temperature monitoring SIL Disabled Minimal temperature: -40°C Maximal temperature: 150 90°C 100°C 110°C 120°C 130°C 140°C 150°C
13	VDD_ENA[1]	1	10	bit	0 1	Monitoring supply voltage SIL Disabled Enabled
11 12	VXPETH[3] VYPETH[3]	8	7:0	decimal	0 255	Good-Fail-Threshold for self-test Range: 0...255, see 14
12	STCYC	6	13:8	decimal	0 .. 63	Self-test cycles
13	FAILTH[2]	8	7:0	decimal	0 255	Error threshold channel monitoring SIL Range: 0...255
11	ST_MODE	1	8	bit	0 1	Self-test mode Disabled Enabled

[1] relevant when SIL_ENA = 1
[2] relevant when CHN_ENA = 1
[3] relevant when ST_MODE = 1 and STCYC > 0

8.5.4 Sensor signal correction and evaluation registers

Table 40: Sensor signal correction and evaluation registers

Register address	Parameter name	Number of bits	Bit position	Format	Value	Description
9	VPO	8	7:0	decimal	0 255	Offset compensation adjustment Range: 0...255 (2VREF .. 0)
18	TC_ENA	1	10	bit	0 1	Digital temperature and characteristic correction Disabled Enabled
24	PTSCALE	4	13:10	decimal	0 .. 7	Digital sensor characteristics correction Scaling factor range: 0...7
17 18 19	PTA_A PTA_B PTA_C	10	9:0	-	-	Digital sensor characteristics correction 2^{nd} order factor (two's complement) Range: -512... +511 * $2^{(-PTSCALE-10)}$
20 21 22	PTB_A PTB_B PTB_C	10	9:0	-	-	Digital sensor characteristics correction 1^{st} order factor (two's complement) Range:: -512...+511 * $2^{(-PTSCALE-1)}$
23 24 25	PTO_A PTO_B PTO_C	10	9:0	-	-	Digital sensor characteristics correction Offset (two's complement) Range: -512...+511
26 27	XENA_FIR YENA_FIR	3	12:10	-	-	FIR-Filter configuration according to channel. See table 13
26 26 27 27	FIR_LEN0 FIR_LEN1 FIR_LEN2 FIR_LEN3	5	9:5 4:0 9:5 4:0	decimal	0 .. 31	FIR-Filter order Range: 0..31
15 16	THRESH0 THRESH1	14	13:0	decimal	0 ... 16383	Reference values for threshold detection Range: 0 … 16383
17	THRESSEL	4	13:10	-	-	Threshold select, see table 14
14	THRES_EN	1	11	bit	0 1	Threshold enable disabled enabled
14	THRES_RES_MAX	2	10:9	decimal	0 .. 4	Number of measurement values suppressed after threshold flags activation, see 6.9.3
14	THRES_MAX	9	8:0	decimal	0 … 511	Number of measurement values suppressed before threshold flags activation, see 6.9.3
3 8	AVGX AVGY	2	13:12	binary	00 01 10 11	Averaging ADC value 00 = disabled 2 value 4 value 8 value

8.5.5 Test-/Special registers

Table 41: Test-/Special registers

Register address	Parameter name	Number of bits	Bit position	Format	Value	Description
0	VTSELX	4	13:10	bit/binary	Bit 3 = 1 Bits (2:0) 000 001 010 011 100 101 110 111	Multiplexer channel X output: at XYCH_OUT VTSELX(3): 1 = enabled and 0 = disabled VTSELX(2:0): 0 = VSSA 1 = SHX 2 = VREF 3 = CHXOUTP 4 = ADCITST 5 = VPTAT 6 = ADINPMON 7 = ADINNMON
4	VTSELY	4	14:10	bit/binary	Bit 3 = 1 Bits (2:0) 000 001 010 011 100 101 110 111	Multiplexer channel Y output: at XYCH_OUT VTSELY(3): 1 = enabled and 0 = disabled VTSELY(2:0): 0 = VSSA 1 = SHY 2 = VSSA 3 = CHYOUTP 4 = RESERVED 5 = RESERVED 6 = RESERVED 7 = RESERVED
6	EEPDATA	14	13:0	binary		EEPROM/SRAM read/write register
9	SH_ENA	1	10	bit	0 1	Sample and hold activation Analogue outputs SH_X and SHY deactivated Analogue outputs SH_X and SHY activated
30	CLKADJ*	5	8:4	-	-	Oscillator cell adjustment
30	EECLKADJ*	5	13:9	-	-	EEPROM oscillator cell adjustment
25	TST	4	13:10	binary	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Multiplexer Test output BUSY 00 = Disabled 01 = ADC_CLK 02 = CONV_ADC 03 = XCLOCK_SW 04 = YCLOCK_SW 05 = XDISCHARGE 06 = YDISCHARGE 07 = XREFSEL 08 = YREFSEL 09 = BUSY_ADC 10 = INPSEL(0) 11 = INPSEL(1) 12 = CLKMX 13 = EECLK 14 = EEPWR 15 = ESTBY
30	VREF*	4	3:0			Reference voltage adjustment
9	PDREF	1	12	bit	0 1	Power down reference voltage Power-Down reference voltage deactivated Power-Down reference voltage activated
9	ADCPD	1	11	bit	0 1	Power down ADC Power-Down ADC activated Power-Down ADC deactivated
29	RAMRWSPI	1	13	bit	0 1	Select Read/Write via SPI/I²C, see Table 23 EEPROM RAM

* Adjustment by manufacturer

9 Contact

AMAC ASIC- und Mikrosensoranwendung Chemnitz GmbH
Kopernikusstr. 16
09117 Chemnitz
Germany

Telefon: +49 371 33 42 04 – 0
Telefax: +49 371 33 42 04 – 69
eMail: info@amac-chemnitz.de
Web: http://www.amac-chemnitz.de